THE INTERNATIONAL MAGAZINE FOR ELECTRONICS ENTHUSIASTS
June 1991 UK £1·75

Elektor Electronics

The QTC loop antenna
Real-time clock for Atari ST
Stepper motor board - Part 1
Universal battery charger
Timecode interface - Part 1

DIGITAL PHASE METER

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ELEKTOR Electronics
The international magazine for electronics enthusiasts

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June 1991
Volume 17
Number 190

Apologies

We regret that owing to circumstances beyond our control the "Timecode interface for slide controller" had to be postponed after this month's front cover had already been printed.

In next month's issue

- **As usual in our July issue, more than 50 small but interesting articles presenting new and practical ideas, concepts, and developments on all aspects of electronics**

PLUS

- Timecode interface for slide controller – Part 1
- Multi I/O for IBM
- Black-and-white video digitizer
- Radio data systems
- Modern LED clock
- Logic analyser - Part 5
- Measurement techniques – Part 6
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- One-shot solid-state relay timer
- 8088 single-board computer

Front cover

This month's project in our measurement series features a digital phase meter. This is a rare instrument, even in the laboratory or workshop of audio and hi-fi engineers. Many engineers and technicians measure phase shift with the aid of an oscilloscope (Lissajous figures). That is not a very accurate method: the phase meter presented is accurate to within 0.5° over the frequency range 10 Hz to 20 kHz.

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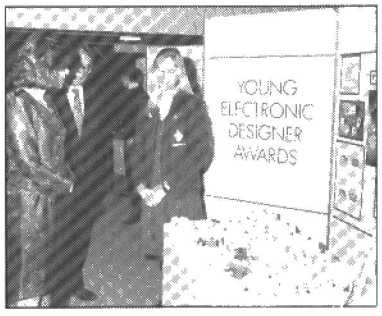
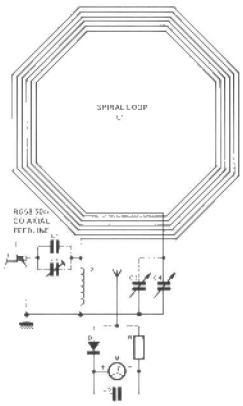


A picture to restore or increase your faith in youth and electronics: this young lady, Polyanna Robinson, who is only 14, won first prize in the Junior Category of the YEDA awards
see page 13



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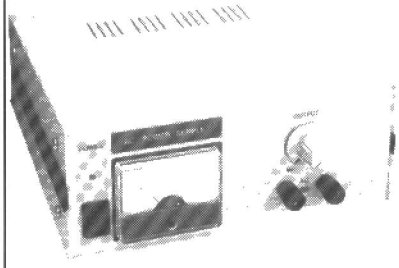

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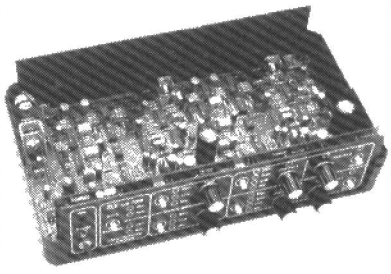

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TELECOMMUNICATIONS AND SAFETY OF HUMAN LIFE

THE DAY after this issue of *Elektor Electronics* reaches the newsstands, Friday 17 May, is World Telecommunication Day, celebrated every year by member countries of the International Telecommunication Union—ITU. It is the date of signature in Paris, in 1865, of the first International Telegraph Convention which set up the International Telegraph Union, the forerunner of today's ITU.

This year, World Telecommunication Day is celebrated as part of the Natural Disaster Prevention Decade proclaimed by the United Nations General Assembly. Other international organizations, whose activities are significantly dependent on telecommunications, have therefore been associated to the celebrations: the International Civil Aviation Organization (ICAO), the International Maritime Organization (IMO), the World Meteorological Organization (WMO), the Office of the United Nations Disaster Relief Co-ordinator (UNDRO), and the League of Red Cross and Red Crescent Societies.

The topic chosen for this year by the Adminstrative Council of the International Telecommunication Union is *Telecommunications and safety of human life*.

Radio was first used to save life at sea in March 1899, when it was used by a lightship to report that the steamer *Elbe* had run aground. It was also in 1899 that the first ship was fitted with radio. Since that time, radiocommunications has proved to be of paramount importance to safety at sea.

In 1912, some three months after the passenger ship *Titanic* disaster occurred with the loss of more than 1500 lives, an international radio conference met in London to review and amend the 1906 International Radiotelegraph Convention which prescribed the distress and calling frequencies, classes of ship service (watchkeeping), ship's radio equipment, and requirements for certification of operators for shiop stations. Later, in January 1914, also in London, an international maritime conference adopted the first International Convention for the Safety of Life at Sea (SOLAS), which required certain ships to carry an MF radiotelegraph installation.

The existing distress system

The subsequent 1929, 1948, 1960 and 1974 SOLAS Conventions all required passenger ships and cargo ships of 1600 tons gross and upwards to carry a radiotelegraph station. It was not until 1948 that requirements for MF radiotelephone stations were included in the convention and then only for ships of between 300 and 1600 tons gross not fitted with an MF radiotelegraph station. Limited requirements for a VHF radiotelephone station for safety of navigation were included in SOLAS in 1974, but it was not until 1981 that requirements for all SOLAS ships to be capable of communicating with each other by VHF and MF radiotelephone were achieved.

Subsequent World Administrative Conferences (WARC) convened by the ITU provided the radiotelephone distress call, radiotelephone distress and calling frequencies, and reduced the distress bands as radio technology and equipment improved.

Until 1960, when IMO came into being, the ITU was solely responsible for all aspects of maritime radiocommunications, including distress and safety radiocommunications. The 1960s saw great changes and improvements in radiocommunication systems, e.g., satellite communications, selective calling, direct-printing telegraphy, etc. Both ITU and IMO recognized the advantages of these systems for improving all maritime radiocommunications.

The existing morse radiotelegraphy and radiotelephone system, with a required MF communication range of 100–150 nautical miles, provided a distress system based, if time permitted, on alerting ships in the vicinity of the distress and coast stations within range. The system therefore did not cover ships that sank suddenly or ships in distress that were too far away from those who could assist.

Improvement of maritime radiocommunications

In February 1966, IMO decided to study the operational requirements for a maritime satellite communication system and in 1967 the ITU WARC invited IMO to continue this work.

In the early 1970s, IMO, in close co-operation with ITU's International Radio Consultative Committee (CCIR), started active preparations for the establishment of a maritime satellite communication system to serve the maritime community. This work resulted in 1979 in the establishment of the International Maritime Satellite Organization INMARSAT.

In 1973, IMO adopted a policy document on the development of the maritime distress system, which outlined the steps that should be taken to gradually improve the existing system and ultimately achieve what was then the distant future system and is now known as the Global Maritime Distress and Safety System (GMDSS).

IMO also sought to improve search and rescue (SAR) world-wide for those in distress at sea and, concurrent with the development of the INMARSAT Convention, prepared the SAR Convention, which was adopted in 1979. Under the convention, SAR is based upon co-ordination of all SAR operations, wherever they occur in the world, by responsible authorities ashore (rescue co-ordination centres (RCCs)). As MF and VHF communications have limited range, in order to enable RCCs to meet their responsibilities under the SAR Convention, ships operating outside the MF range need a long-range HF or satellite communication capability. →

Produced and published by **ELEKTOR ELECTRONICS (Publishing)**

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LONDON SW18 4JQ
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or +44 81877 1688 (*International*)
Telex: 917003 (LPC G)
Fax: 081-874 9153 (*National*)
or +44 81874 9153 (*International*)

Advertising: PRB Limited
3 Wolseley Terrace
CHELTENHAM GL50 1TH
Telephone: (0242) 510760
Fax: (0242) 226626

Subscriptions:
World Wide Subscription Service Ltd.
Unit 4, Gibbs Reed Farm
Pashley Road
TICEHURST TN5 7HE
Telephone: (0580) 200657 (*National*)
or +44 580 200 657 (*International*)
Telefax: (0580) 200616 (*National*)
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Postbus 75
6190 AB BEEK
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Fax: +31 46 37 01 61
Managing Director: M.M.J. Landman

Distribution:
SEYMOUR
1270 London Road
LONDON SW16 4DH

Printed in the Netherlands by NDB, Zoeterwoude

Overseas editions:
FRANCE
Elektor sarl
Les Trois Tilleuls
B.P. 59; 59850 NIEPPE
Editors: D.R.S. Meyer;G.C.P. Raedersdorf
GERMANY
Elektor Verlag GmbH
Süsterfeld Straße 25
5100 AACHEN
Editor: E.J.A. Krempelsauer
GREECE
Elektor EPE
Kariskaki 14
16673 Voula - ATHENA
Editor: E. Xanthoulis
INDIA
Elektor Electronics PVT Ltd
Chhotani Building
52C, Proctor Road, Grant Road (E)
BOMBAY 400 007
Editor: C.R. Chandarana
ISRAEL
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P O Box 41096
TEL AVIV 61410

Publisher: M. Avraham
NETHERLANDS
Elektuur BV
Peter Treckpoelstraat 2–4
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Editor: P.E.L. Kersemakers
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Publisher: Edward T. Dell

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Development of the GMDSS

The advent of INMARSAT enabled the development of the GMDSS through a carefully considered integration of satellite and modern terrestrial radiocommunication techniques and procedures. Development of the GMDSS required very close co-operation between ITU and IMO. In general, IMO are developing the operational requirements, while the ITU through CCIR recommend the technical specifications of the equipment and procedures for its use.

In the late 1970s, several countries, particularly the United States and the USSR, began experiments with satellites that resulted in the COSPAS-SARSAT system being established well before implementation of the GMDSS. Since that time, the system has provided a significant contribution to SAR operations and has assisted in saving hundreds of lives.

In the later 1970s, IMO, in co-operation with IHO, established the world-wide navigation warning service (WWNWS) for the co-ordination and broadcast of navigational warnings to ships. Since 1929, Contracting Governments to the SOLAS Convention have undertaken to broadcast meteorological warnings and forecasts to ships and to make arrangements for the reception of danger warnings and meteorological reports, co-ordinated by WMO through its world weather watch (WWW), from ships. These matters, together with broadcasts of SAR and other urgent information, provide the maritime safety information (MSI) element of the GDMSS.

The GDMSS will be fully implemented in 1999 when, except possibly for a few remaining stations, use of morse radiotelegraphy by ships will cease after 100 years of dedicated and faithful service.

The concept of the GDMSS is based on the use of the most up-to-date radiocommunication technologies to provide a comprehensive distress and safety system of communication between ships and between ships and the shore and vice versa wherever in the world the ships may be situated. The functional requirements of the GMDSS include transmitting and receiving ship-to-shore and shore-to-ship distress alerts, ship-to-ship distress alerts, SAR co-ordinating communications, on-scene communications, signals for locating, maritime safety information (MSI), general radiocommunications, and bridge-to-bridge (navigational) communications.

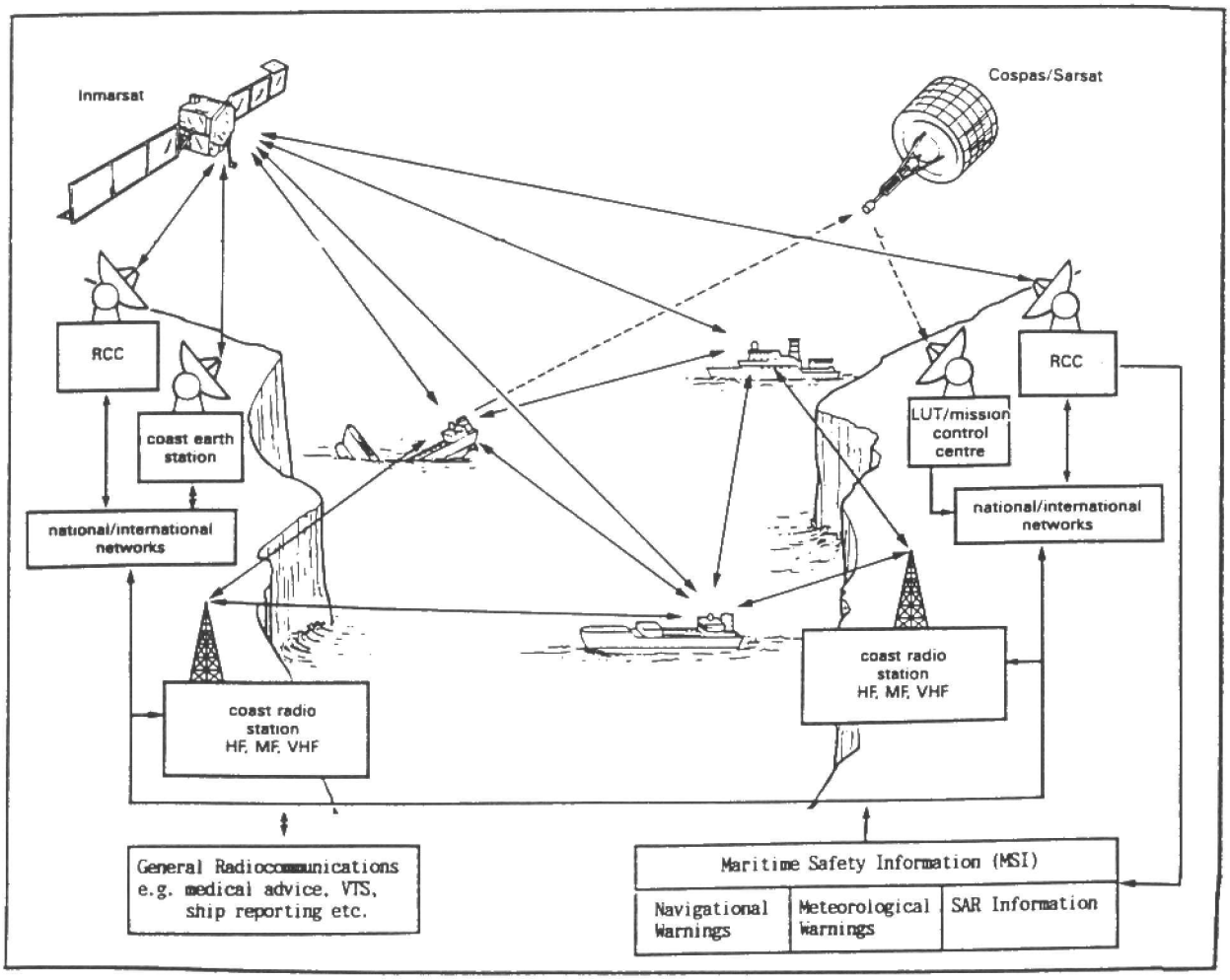
Implementation of the GMDSS

Implementation of the GMDSS will be phased to allow for equipment redundancy:

1. all ships to be fitted with a NAVTEX receiver and satellite EPIRB by 1 August 1993;
2. all ships constructed before 1 February 1992 to be fitted with a radar transponder and two-way radiotelephone apparatus for survival craft by 1 February 1995;
3. all ships constructed after 1 February 1995 to comply with all appropriate requirements for the GMDSS;
4. all ships to be fitted with at least one radar capable of operating in the 9 GHz band by 1 February 1995;
5. all ships to comply with the appropriate requirements for the GMDSS by 1 February 1999.

Emergency distress alerting capability

A distress alert capability in case the ship sinks suddenly or the radio station is destroyed is provided by a satellite emergency position-indicating radio beacon (EPIRB) that is capable of floating free from the sinking ship and being automatically actuated and transmitting the ship's identity and either its position (INMARSAT) or a signal that provides the ship's position (COSPAS-SARSAT). The satellite EPIRB is portable and can be carried into survival craft, which will also be equipped with portable VHF transceivers, on-scene communications and search and rescue radar transponders (SARTs) for final location by SAR units arriving at the distress position. ■



General concept of the GMDSS

RESULTS OF THE 1991 YOUNG ELECTRONIC DESIGNER AWARDS

HRH The Duchess of York presented the 1991 Young Electronic Designer Awards on 3 April at the Science Museum, London. The Senior Category was won by Stephen Brown of the Royal Naval Engineering College, Plymouth; the Intermediate Category was won by Jonathan Saville of the Queen Elizabeth Grammar School, Wakefield; and the Junior Category was won by Polyanna Robinson of The Godolphin School, Salisbury.

The Texas Instruments' Prize of £2,500 for the most commercially viable project was awarded to Polyanna Robinson.

The Mercury Communications 'Planet Award', also worth £2,500, for the most environmentally and socially aware technology went to Jonathan Saville.

The Duchess praised the work of all 21 finalists, saying how much she admired their ingenuity and their understanding of the science of electronics. The 21 young designers, whose ages ranged from 12 to 24, came from 15 different educational establishments in all parts of the UK.

YEDA is sponsored jointly by Texas Instruments Ltd and Mercury Communications Ltd. Ken Sanders, managing director of TIL, said: "A venture like YEDA requires a commitment of years, rather than days. Sponsorship is more than just signing cheques. Sponsors should also try to provide ideas and dynamism which will contribute to the *life* of the venture. This is why we are finding ways in which completed YEDA projects can be given a much wider audience among the general public".

Peter van Cuylenburg, Mercury's chief executive, added: "Mercury's co-sponsorship of the YEDA awards and the introduction of the Planet Award underline our determination to encourage new talent and our concern for the well-being of our planet. By donating this award, we hope to encourage the development of safer and environmentally sympathetic technology". ■

HRH The Duchess of York and Professor John Eggleston, Chairman of the YEDA Board of Trustees, disuss Pollyanna Robinson's Quizmaster. This device, which indicates the first contestant to respond to a question in a game, earned Polyanna (14) first place in the Junior Category.

Jonathan Saville (16) discusses his project, an electronic automated self-contained river water pollution monitor, with HRH The Duchess of York.

First place in the Senior Category went to Stephen Brown (24), who developed a system that interactively displays images from the AutoCad design package.

EVENTS

IEE AND IEEIE PROGRAMME

3 June—Inspection and testing of electrical installations.
4 June—Loud and clear– obtaining intelligible public address at stations.
5 June—Transparent optical networks in Europe.
5 June—High frequency resonant power supplies.
10 June—Testing tomorrow's technology today.
10–12 June—Reliability '91. International conference at the Royal Lancaster Hotel, London. Details from R. Matthews, AEA Technology, Wigshaw Lane, Culcheth, Warrington WA3 4NE, (0925) 31244.
11 June—Broadcasting traffic information.
12 June—Practical methods for robust control system design.
12 June—Satellite antenna technology for the 21st century.
14 June—Software in air traffic control systems.
14 June—National Library of Scotland – phase 1: electrical system and lighting.
17 June—Electronic CADMAT in teaching.
17 June—16th Edition – IEE wiring regulations.
20–22 June—Television measurements (Fourth International Conference, Montreux).
21 June—Embedded software control systems.
24 June—Measurement uncertainties for Europe – is there a common approach?
27 June—Electromagnetic compatibility for project engineers.

Information on these, and many other, events may be obtained from the IEE, Savoy Place, London WC2R 0BL, Telephone 071 240 1871 or the IEEIE, Savoy Hill House, Savoy Hill, London WC2R 0BS, Telephone 071 836 3357.

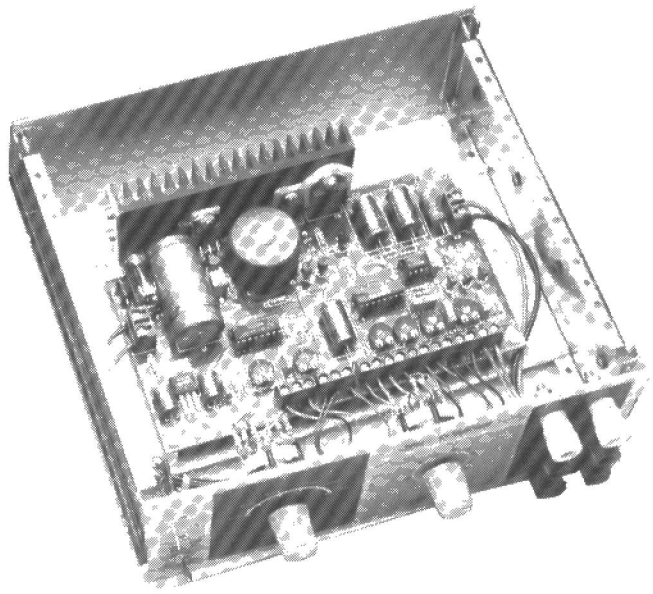
An easy-to-use character generator, cable communal systems, an in-line recording console and a newsroom autocue are among many new products that will feature on the stands of more than 40 British companies taking part in the **TV Symposium and Exhibition** in Montreux from 13 to 18 June. The group is being organized by the Electronic and Business Equipment Association in co-operation with the Department of Trade and Industry. In addition, the Association will mount an information stand where any enquiries about the exhibits or the industry may be directed.

Details from the Department of Trade and Industry, 1–19 Victoria Street London SW1H 0ET; telephone 071 215 5000.

This month, Frost & Sullivan will conduct seminars on **ISDN Protocols and implementation**; **An introduction to telecommunications**; the **OSI reference model**; **X.25 and packet switching networks**; **Digital cellular telephony**; **What's new in IBM's SNA?**; and **Advanced packet switching**.

Details from Frost & Sullivan, Sullivan House, 4 Grosvenor Gardens, London SW1W 0DH, Telephone 071 730 3438.

UNIVERSAL Ni-Cd BATTERY CHARGER



by A. Rigby

Ni-Cd batteries are now used in so much everyday equipment that most households need at least one suitable charger. The one presented here can be used to charge virtually all current Ni-Cd batteries.

THE charger is based on the Telefunken Type U2400B processor, which has been specially developed for this application. This device contains most of the logic circuits necessary for automatically controlling the charging of Ni-Cd batteries.

Initially, charging takes place during a predetermined period of time, after which trickle charging takes over. The trickle charging, which may continue for long periods of time, ensures that the battery capacity does not degrade during the life of the battery.

The charger has a number of safety features. For instance, if the temperature of the battery becomes too high or when the e.m.f. of the battery rises above a certain (predetermined) value, the charging cycle is discontinued immediately. The processor then assumes its stand-by mode and remains there until the temperature or the e.m.f. drops below its limiting value.

A flow diagram of the charging process is given in Fig. 2. After the battery has been connected and the start reset operated, the processor first arranges for the battery to be discharged. During the discharge cycle, the temperature of the battery ($T<T_{max}$) and its e.m.f. ($U<U_{min}$) are monitored continually. When the e.m.f. drops to the level of U_{min}, the processor assumes that the battery has been discharged completely, and sets its discharge register. The circuit then switches to the charging mode. During charging the lapsed charging time is compared with the preset charging time ($t>t_{max}$) and the e.m.f. with the maximum (preset) voltage ($U>U_{max}$). Furthermore, the content of the discharge register and the battery temperature are monitored constantly. At the end of the preset charging time ($t>t_{max}$), the charging cycle is terminated and the processor actuates the trickle charging mode.

As already mentioned, if during charging one of the preset parameters is exceeded, charging is discontinued. At the same time, the status of the error register is increased by 1 and reread. If no error occurred previously, the status of the counter after the present error will be smaller than 2($Z<2$). If the counter status is smaller than 2, the e.m.f. and temperature of the battery are checked once again; if these are all right, the charging process is continued. If the content of the error register is greater than, or equal to, 2, charging is continued or stopped, depending on the position of a switch as explained later.

As is seen in Fig. 1, the processor needs only a few external components to perform the functions discussed so far. During the discharge cycle, the e.m.f. of the battery is monitored via U_{min} (pin 6). In this, use is made of a switchable voltage divider, R_{35}–R_{43}-R_3–P_2, which attenuates the battery voltage. During the discharge cycle, output DIS(charge) (pin 10) is active and high. The discharging is assumed complete when the voltage level at pin 6 drops below the level (0.53 V) of the internal reference voltage.

During charging, output LOAD (pin 12) becomes active and high; the battery voltage is then applied to pin 4 (U_{max}) via potential divider R_{35}–R_{43}-R_2-P_1. If the voltage at pin 4 is higher than the internal reference potential, the processor switches to the stand-by mode.

Since it is important for the user to know in which state the processor is, two LEDs are driven via STATUS output pin 9. Table 1 shows the operation of these diodes in the various modes.

A reference voltage of 3 V (nominal) is applied to pin 7, the PWM input, switch S_1, network R_4-C_2, voltage divider R_5-R_6 and the two series-connected LEDs.

Series combination R_4–C_2 at the input of the internal oscillator, pin 3, is a frequency-determining network .

Monitoring of the battery temperature is accomplished by R_6, which has a negative temperature coefficient. The potential at junction R_5–R_6 is monitored via input U_{temp} (pin 5). The charging process is stopped when the battery temperature reaches 40 °C; the resistance of R_6 is then about 440Ω.

The position of switch S_1 determines the selection made by the processor when two or more errors in the charging process have been signalled. If the switch is connected to the reference voltage, charging is continued even when two (but no more) errors have occurred; if it is connected to earth, however, full charging is discontinued and trickle charging commenced.

The charging time is preset via the TIME input, pin 13. When the internal 200 Hz oscillator is used, a high level at pin 13 sets the charging time to 1 hour. When the pin is connected to earth (low level), the charging time is 30 minutes.

The timer may also be driven by an ex-

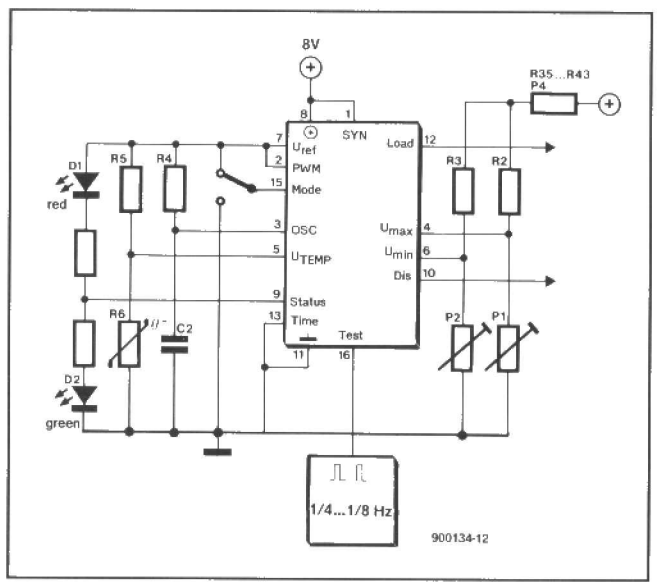


Fig. 1. Basic circuit for the U2400B processor.

Table 1

D_1	D_2	S_1	Function
(red) on	(green) off	x	no battery connected; battery faulty or battery flat
flashes	off	x	discharge cycle
off	flashes	x	charging cycle
off	on	x	trickle charge mode
flashes	flashes	E	charging continues after two errors
on	off	D	trickle charging after two errors

x = irrelevant
E = connected to U_{ref}
D = connected to earth

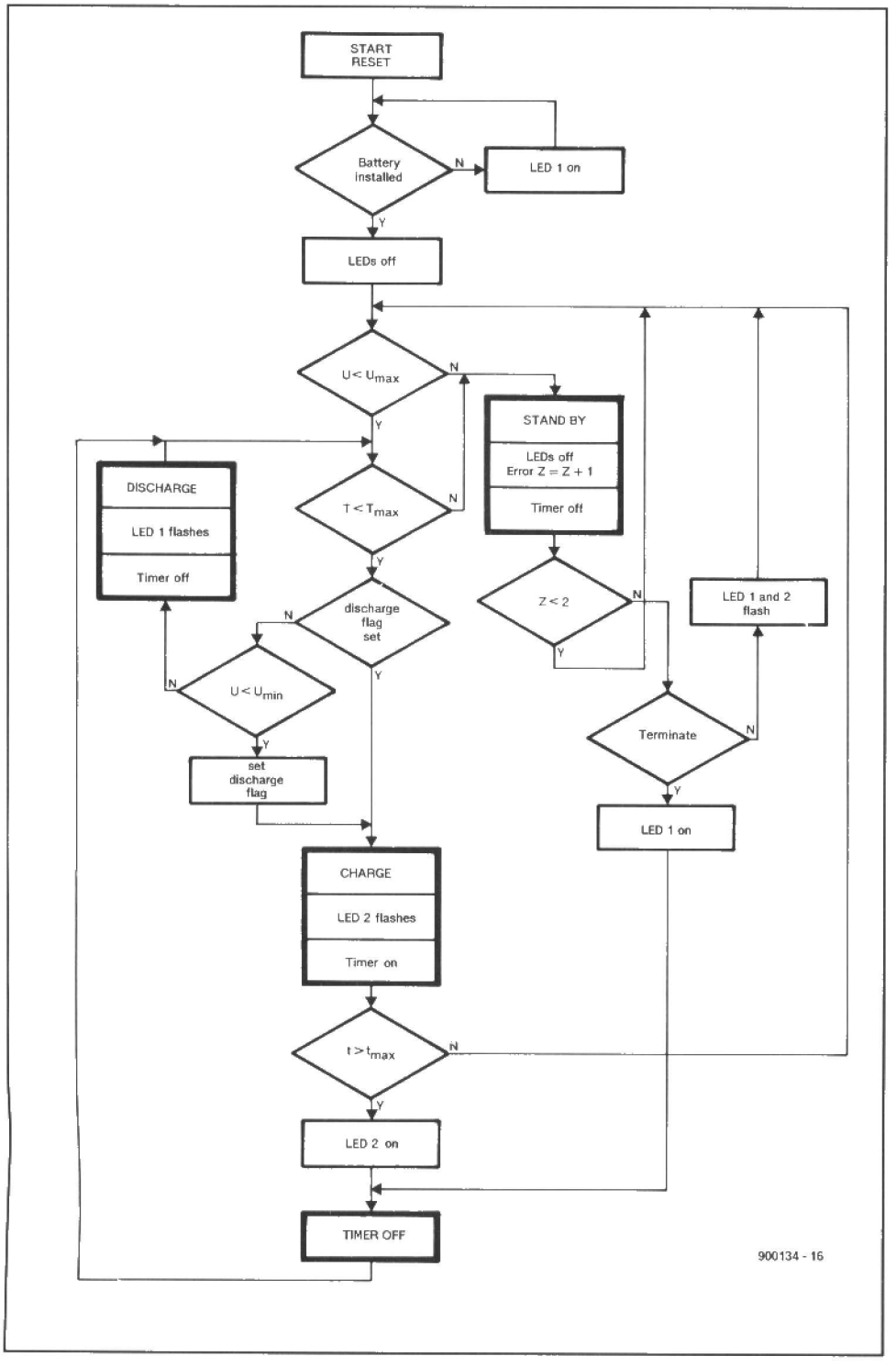


Fig. 2. Flow diagram of the battery charger.

ternal clock, connected to pin 16; pin 13 must then be earthed. The internal 200 Hz oscillator then provides the clock signals for the remaining functions of the processor. A frequency of 0.5 Hz at pin 16 sets the charging time to 1 hour; halving that frequency doubles the time. An external clock based on a 4060 IC as shown in Fig. 8 can provide frequencies down to 0.125 Hz, which would give a charging time of 4 hours.

Charging

In a practical charger, the processor does not drive a simple transistor, but a fairly complex current source, controlled as shown in Fig. 3. The charging current flows through R_{22}, resulting in a potential drop across this resistor that is directly proportional to the charging current:

$$U_{R22} = I_{load} R_{22}.$$

This voltage is used for controlling the charging current. Note that the negative battery voltage, U_{bat}, is in reality more positive than the supply voltage, U_V, because the positive terminal of the battery is connected to a second, higher supply voltage.

Since transistor T_5 is connected as a diode, the emitter of T_6 is connected to U_V at all times. Therefore, the potential drop across the emitter resistor, R_e, which is the quivalent of R_{29}–R_{34}–P_6 in Fig. 8, is exactly the same as that across R_{22}:

$$U_{Re} = U_{R22} = I_{Re} R_e.$$

As an example, assume that $R_{22} = 0.1\ \Omega$, $I_{load} = 1$ A, and that a current of 1 mA is required through the transistor. The drop across R_{22} is 100 mV, so that

$$R_e = 100\times10^{-3}/10^{-3} = 100\ \Omega.$$

Since the emitter current is now known, the voltage drop across the collector resistor is:

$$U_{Re} = 1.2\times10^{3}\times10^{-3} = 1.2\ \text{V}.$$

This makes it clear that a change in the charging current results in a change in the voltage at F_B. That voltage may, therefore, be used for the control of a regulatory circuit in a switch-mode power supply.

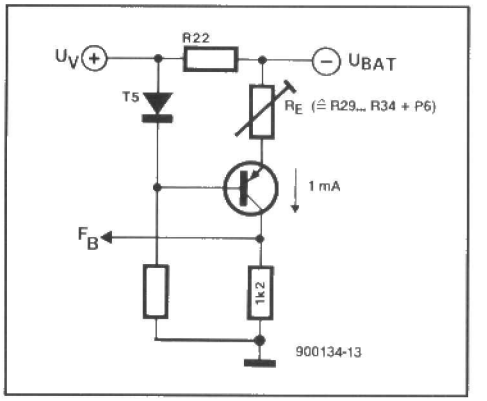


Fig. 3. Part of the circuit controlling the charging current.

Switch-mode power supply

A switch-mode power supply is used to enable the charger to cater for the simultaneous charging of, say, up to ten batteries; a conventional mains supply could be used, but the dissipation in this will be quite large when only a few batteries are being charged.

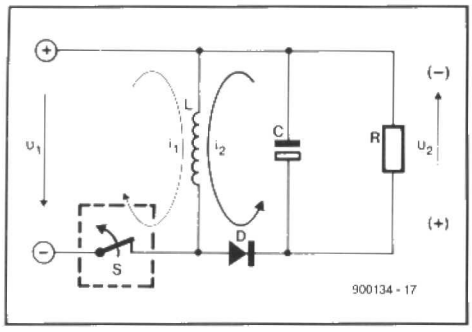


Fig. 4. Concept of a switch-mode power supply.

The basic operation of such a supply is shown in Fig. 4. Electronic switch S is switched on and off by electrical circuits. When it is closed, a current i_1 flows from the ⊕ supply terminal to earth via inductor L, resulting in a magnetic field around the inductor. Diode D is switched off and capacitor C, therefore, has no influence on the circuit, although it can discharge via load resistance R (representing the batteries to be charged).

When S is opened, the self-inductance of L causes a current i_2 in the opposite direction from i_1 and this charges C via the diode.

The level of output voltage U_2 depends on the properties of the inductor, the switching logics and the on-off ratio of the switch. In the present charger, a commercial inductor is used: it is not advisable to wind this yourself.

The circuit of the supply used is shown in Fig. 5. It is based on Linear Technology's Type LT 1070. A 40 kHz oscillator provides a train of rectangular pulses that are used to switch a transistor via a driver stage. The duty factor is determined primarily by the output voltage of the (differential) error amplifier.

The collector voltage of T_6 is 1.2 V when the regulator is in a stable condition. Because of its internal reference voltage of 1.24 V, the error amplifier then has no effect on the switching behaviour of the output transistor. When the charging current increases to too high a level, U_c rises, and the output of the error amplifier goes low. This results in an alteration of the on-off ratio of he transistor, which lowers the charging current.

Zener diode D_6 limits the voltage to 18 V.

Discharging

The discharge circuit shown in Fig. 6 has some points in common with the circuit in Fig. 3. Again, use is made of the voltage drop across emitter resistor R_{22}. The supply voltage and the battery voltage have, of course, changed places, since the discharge current flows into a different direction from the charging current.

The non-inverting input of the comparator in the collector circuit of T_3 is held at 2.7 V by zener diode D_3.

The value of R_{14} is determined by the collector current (1 mA) and the reference voltage:

$$R_{14} = 2.7/10^{-3} = 2.7\ k\Omega.$$

The connected batteries are discharged via R_{22} and T_8, which, with T_7, forms a darlington at the output of the comparator.

Voltage monitoring

The processor continually monitors the battery voltage via its pins 4 and 6. Since these inputs measure the voltage with respect to earth and the negative terminal of the battery is connected to the ⊕ supply rail, a simple circuit like that in Fig. 1 can not be used. This means that the battery voltage must be converted so that it *can* be measured with respect to earth.

To this end, a network as shown in Fig. 7 is used. The entire battery voltage is dropped across the emitter resistance, R_e, consisting of resistors R_{35}–R_{43}—see Fig. 8. Since R_e has a value of 1 kΩ per connected battery, the collector current, I_c, through T_1 is

$$I_c = n \times U_z / n \times R_e = U_z / R_e,$$

where U_z is the zener voltage.

When the batteries are charged, the collector current is $1.45/10^3 = 1.45$ mA, and the voltage drop across R_1 and potential dividers R_2–P_1 and R_3–P_2 is 1.74 V. This voltage has the correct polarity with respect to earth. The correct operating point is set with the two potentiometers: how many batteries are connected to the charger is then no longer of importance.

The complete circuit

Large parts of the diagram in Fig. 8 have already been discussed. Note that the switch-mode power supply operates only if pin 1 of the LT 1070 is connected to earth via the LOAD output of the processor and T_4.

Since the resistors at like positions of S_{4a} and S_{4b} have the same value, the discharge and charging currents of batteries are iden-

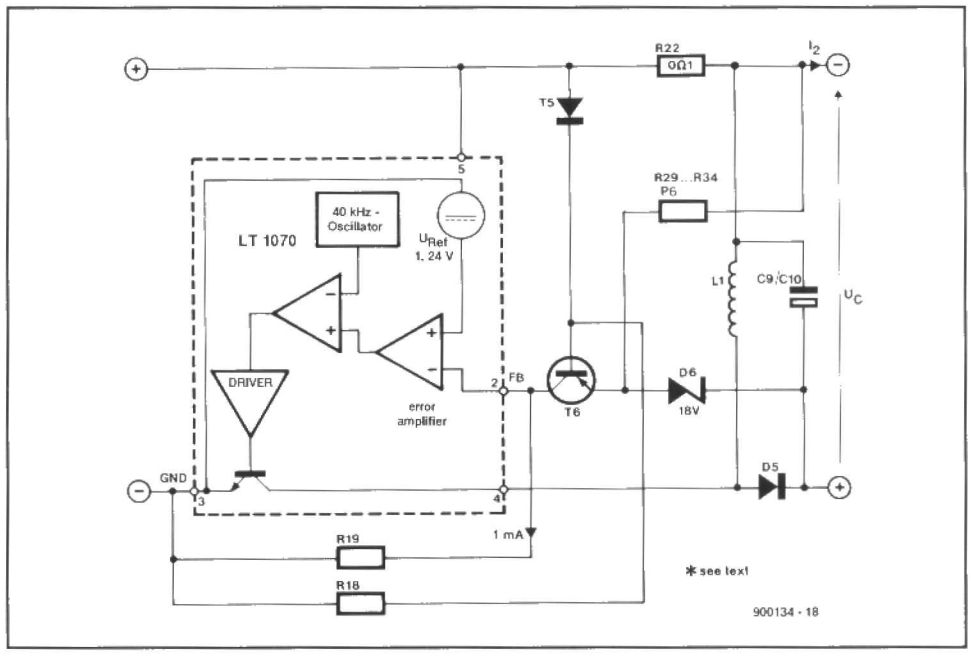


Fig. 5. The switch-mode power supply – see also Fig. 8.

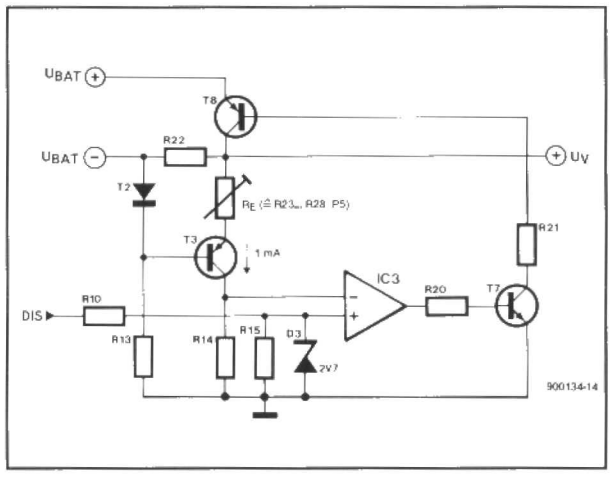


Fig. 6. Circuit for controlling the discharge current. The Dis output of the U2400B provides the reference voltage for IC3.

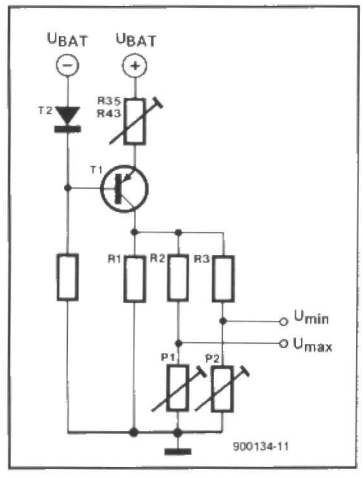


Fig. 7. Circuit for measuring the battery voltage with respect to earth.

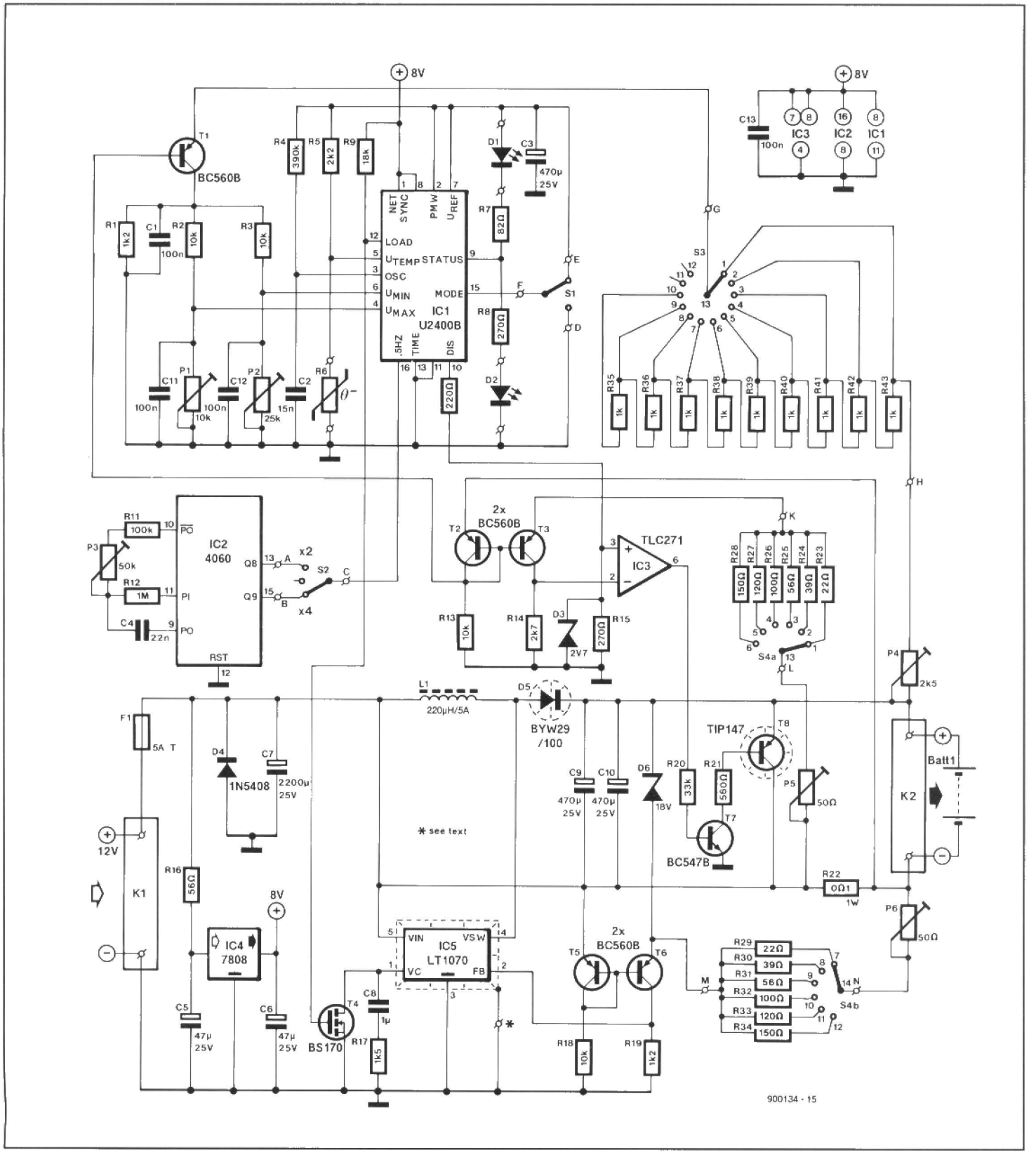


Fig. 8. Complete circuit diagram of the Ni-Cd battery charger.

tical. It is, of course, essential that switch S_3 is set to the correct number of connected batteries (maximum 10).

Switch S_1 selects the mode to be used when one or two errors are detected during the charging process—see Table 1.

When S_2 is in its centre position, the processor uses the standard time setting (of charging) of 1 hour. Its pin 13 is then connected to earth. If this meets all your requirements, the external clock generator consisting of the 4060 (IC_2), R_{11}, R_{12}, C_4, P_3, and S_2, may be omitted.

Otherwise, R_{11}, R_{12}, P_3, and C_4, set the frequency of the oscillator in the 4060 at 100–150 Hz. The divider on board the 4060 provides the required signal frequencies at outputs Q_8 and Q_9. The charging times of 2 and 4 hours respectively associated with these frequencies enable U7 and U11 size batteries to be charged in accordance with manufacturers' specifications.

Preset P_3 enables the correct setting of 2-hour (position A) and 4-hour (position B) charging periods. Should that not be possible, the value of C_4 may be increased (longer periods) or reduced (shorter periods). If a standard time of 30 minutes is wanted instead of 1 hour (S_2 in centre position), disconnect pin 13 of the U2400B from earth.

If C_4 is replaced by a 10 nF type, periods of 30 minutes (S_2 in centre position), 1 hour (S_2 in position A), and 2 hours (S_2 in position B), may be selected

For trickle charging the normal charging circuit is used, but the on-off ratio is ar-

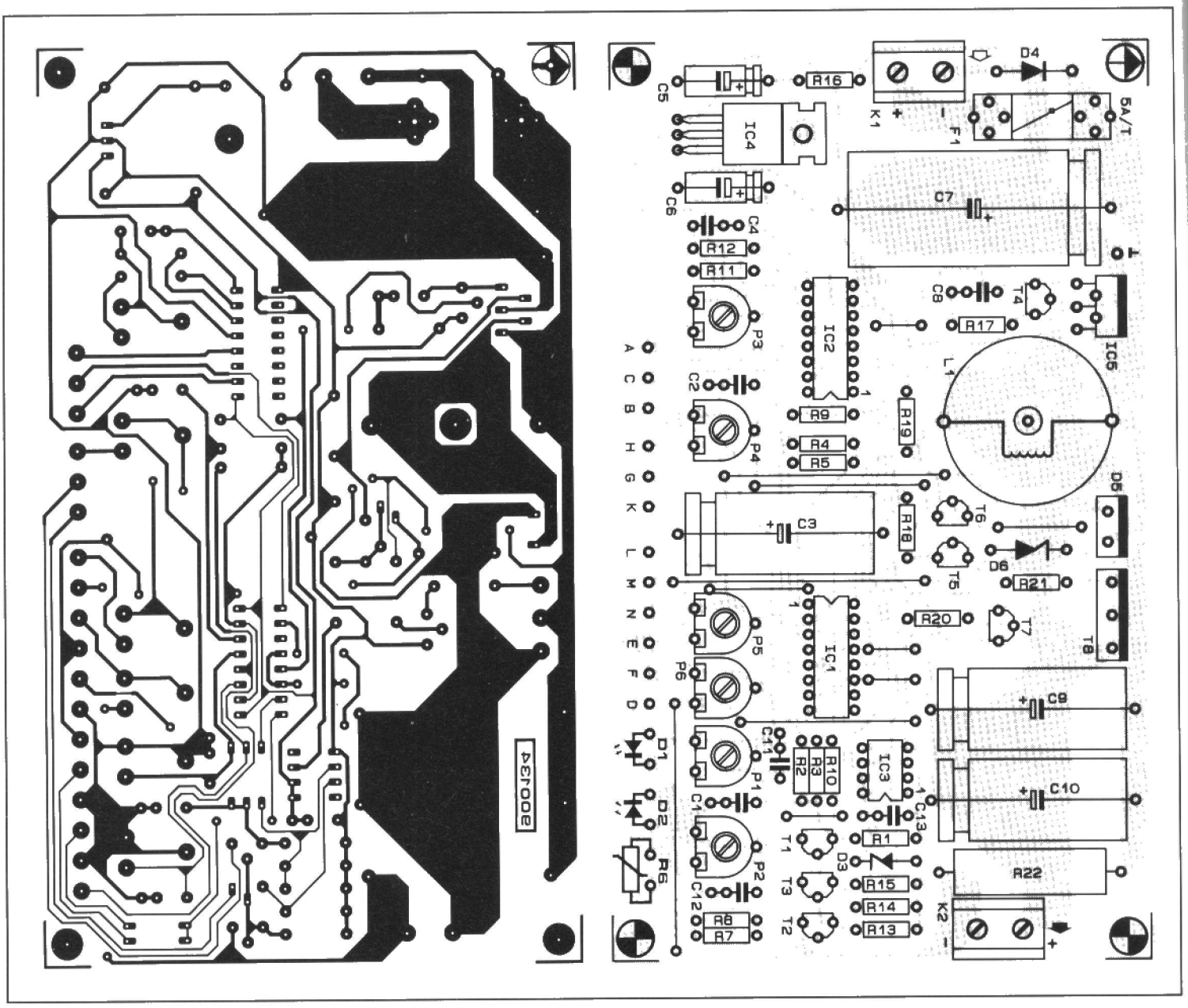


Fig. 9. Component layout and mirror image of track layout of the printed-circuit board for the Ni-Cd battery charger.

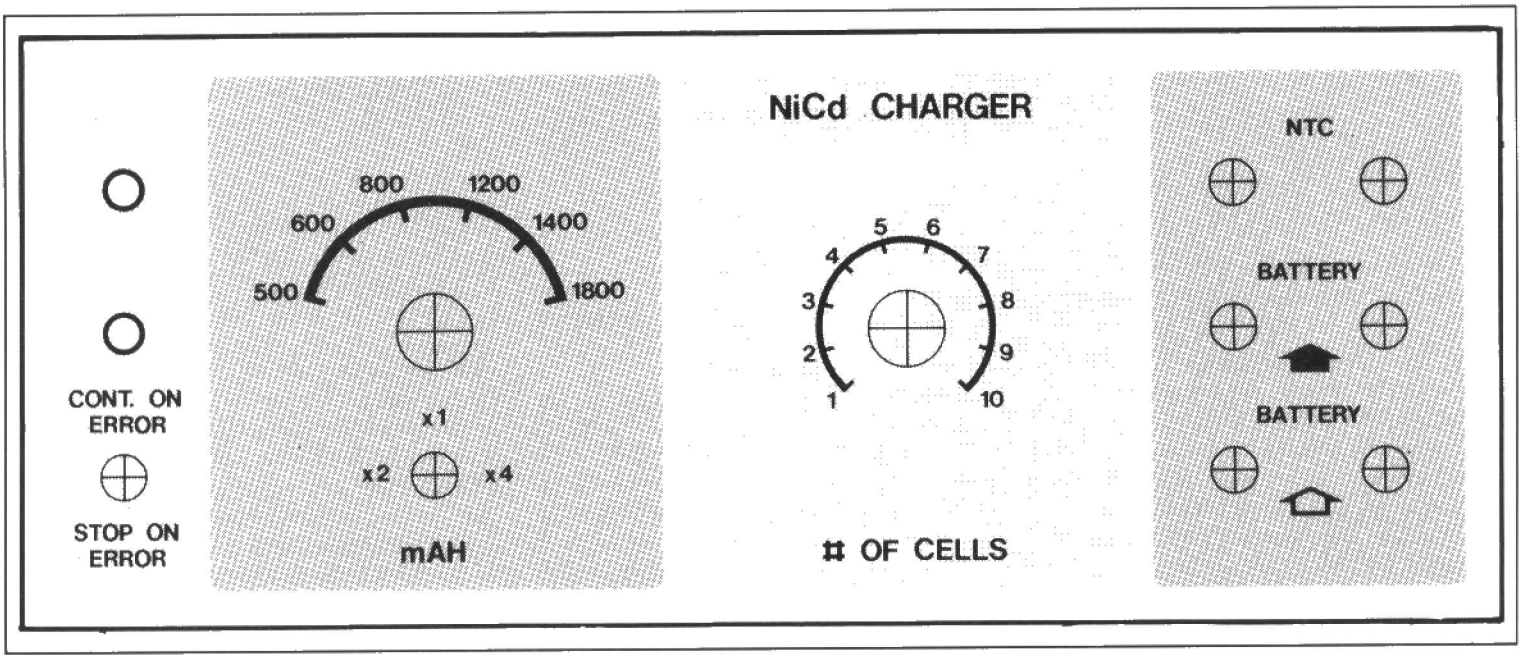


Fig. 10. A front panel foil for the battery charger (196×77 mm) is available through our Readers' Services.

ranged at 1:179, which reduces the average charging current of 1800 mA to 10 mA.

The level of the discharge and charging currents is independent of the selected charging period and may be set to six fixed values with S_4. If it is required for a battery to be charged completely in 30 minutes, the charging current selected must have twice the value of the battery capacity. The charging current in mA corresponds to the capacities shown on the front panel—see Fig. 10. That is, in position 500 mAh, the charging current is 500 mA. Independent of this, the charging current may be doubled by shunting R_{22} with a second 0.1 Ω, 1 W, resistor. This may, however, be done only if the total consumption, $I_{load} \times U_{load}$ does not exceed 25 W, otherwise the switched-mode power supply may become overloaded. Furthermore, the maximum current through the inductor, the fuse rating (max. 8 A), and the maximum discharge current (max. 10 A) must be observed.

Construction

The battery charger is best constructed on the printed-circuit board shown in Fig. 9.

Pay good attention to the polarity of a number of components and make sure that firm solder connections are made where large currents are likely to flow.

The components that need cooling, i.e., IC_5, D_5, and T_8, are located at the edge of the board to enable them to be fitted direct to a suitable heat sink (≥3.2 K W^{-1} at a consumption of ≤25 W).

Make sure that the rear of the LT1070 is electrically bonded to the earth connection specially provided between the supply connections for C_7 and IC_5.

All presets are conveniently grouped at one side of the board.

Resistors R_{23}–R_{43} are not located on the board, but are soldered direct to the rotary switches. These switches are intended to be fitted to the front panel. Their sections that must be connected to the board are marked G/H, K/L, and M/N.

The sockets for connecting the NTC resistor, R_6, the supply (K_1) and the batteries (K_2) are located at the right-hand side of the front panel.

Calibration

There are quite a few calibrations to be carried out, but fortunately they are not very critical. In the first place, do not yet fit IC_1.

1. Set S_4 to 500 (mA), S_3 to 8 (batteries), S_2 to its centre position, and all presets to the centre of their travel.
2. Connect a 12 V, 2 A supply to K_1 (observe polarity!).
3. Connect an auxiliary supply of 8 V to K_2 (observe polarity!).
4. Connect a multimeter between the ⊕ pin of K_2 and point G on the board, and adjust P_4 until the measured voltage is *exactly* the same as that between the pins of K_2.
5. Set S_3 to position 10 and adjust P_2 until with an auxiliary voltage of 8–8.5 V on K_2, a voltage of 0.53 V is measured between junction P_2–R_3–C_{12} and earth. This ensures that all batteries are first discharged to an e.m.f. of 0.8–0.85 V.
6. Set S_3 to position 10 and adjust P_1 until with an auxiliary voltage of 10× the maximum specified (by manufacturer) cell voltage on K_2, a potential of 0.53 V is measured between junction P_1–R_2–C_{11} and earth. The maximum cell voltage is normally about 1.65 V, but may vary from 1.55 V to 1.7 V.
7. The external clock is adjusted with the aid of P_3 and this is best done on an oscilloscope. The frequency of the signal at pin 6 of IC_2 must be 1 Hz. If you have no oscilloscope, use a logic tester with LED indication: the flashing of the LED may be compared with the second hand of a watch.
8. Remove the auxiliary voltage from K_2, switch off the supply voltage, and fit IC_1 and R_6. In an emergency, a normal 1 kΩ resistor may be used for R_6.
9. Connect a partially discharged 500 mAh battery to K_2, set S_4 to 500 and S_3 to 1.
10. Reconnect the 12 V supply to K_1, whereupon the red LED will come on.
11. Connect a digital multimeter (set to 1–2 A d.c.) in series with the battery. About 2 seconds after the connection with the battery is made, the red LED goes out and discharging of the battery begins. Adjust P_5 till the multimeter reads 500 mA.
12. After a little while, the battery will be discharged and charging will commence, indicated by the coming on of the green LED. The current through the multimeter will then change direction: adjust P_6 until it has a value of 500 mA.
13. The battery charger is now ready for use.

Finally

Before charging is begun, always set the various switches to the correct position. The charger can then be switched on and the batteries connected to it. When a different set of batteries or battery is connected to the charger, reset the processor by briefly switching off the supply. ■

PARTS LIST

Resistors:
R1, R19 = 1.2 kΩ
R2, R3, R13, R18 = 10 kΩ
R4 = 390 kΩ
R5 = 2.2 kΩ
R6 = 1 kΩ NTC
R7 = 82 Ω
R8, R15 = 270 Ω
R9 = 18 kΩ
R10 = 200 Ω
R11 = 100 kΩ
R12 = 1 MΩ
R14 = 2.7 kΩ
R16, R25, R31 = 56 Ω
R17 = 1.5 kΩ
R20 = 33 kΩ
R21 = 560 Ω
R22 = 0.1 Ω, 1 W
R23, R29 = 22 Ω
R24, R30 = 39 Ω
R26, R32 = 100 Ω
R27, R33 = 120 Ω
R28, R34 = 150 Ω
R35–R43 = 1 kΩ
P1 = 10 kΩ preset
P2 = 25 kΩ preset
P3 = 50 kΩ preset
P4 = 2.5 kΩ preset
P5, P6 = 50 Ω preset.

Capacitors:
C1, C11, C12, C13 = 100 nF
C2 = 15 nF
C3, C9, C10 = 470 µF, 25 V
C4 = 22 nF
C5, C6 = 47 µF, 25 V
C7 = 200 µF, 25 V
C8 = 1 µF

Inductors:
L1 = choke 200 µH, 5 A

Semiconductors:
D1 = LED, red
D2 = LED, green
D3 = zener, 2.7 V, 400 mW
D4 = 1N5408
D5 = BYW 29/100
D6 = zener, 18 V, 400 mW
T1, T2, T3, T5, T6 = BC560B
T4 = BS170
T7 = BC547B
T8 = TIP147
IC1 = U2400B
IC2 = 4060
IC3 = TLC271
IC4 = 7808
IC5 = LT1070

Miscellaneous:
S1 = miniature C/O switch
S2 = miniature C/O switch with centre position
S3 = rotary switch, 1 pole, 12 positions
S4 = rotary switch, 2 poles, 6 positions
F1 = fuse, 5 A, complete with holder
K1, K2 = 2-way terminal block
Heat sink, 100×38×15 mm
PCB 900134
Front panel foil 900134-F

Estimated cost: £45–£55

LOGIC ANALYSER - PART 4

by K. Nischalke and H.J. Schulz

In this penultimate instalment of the article (which was delayed by circumstances beyond our control), the power supply and the interfaces for the IBM and Atari are discussed, and that completes the hardware for the logic analyser. In the final instalment, the necessary software will be introduced.

THE DESIGN of the power supply is not revolutionary and yet it is unconventional, because the analyser, owing to the number of fast logic circuits, consumes quite a lot of power. The circuit diagram of the power supply is given in Fig. 16.

So as to keep the supply relatively simple and compact, five low-power voltage regulators, instead of one heavy-duty type, are used: one for each board contained in the analyser. This design has the advantage that when a certain board is not used, its supply can also be omitted. Furthermore, the cooling becomes a lot easier.

The supply consists of two independent sections, of which the main one is based on transformer Tr_2, bridge rectifier D_2–D_5, and voltage regulators IC_{65}–IC_{69}. The section based on Tr_1, bridge rectifier D_6–D_9, and regulators IC_{70} and IC_{71} is is intended for probes that can cope with input voltages up to ±12 V. If such a probe is not envisaged, this section may simply be omitted.

Mains transformer Tr_2 is rated at 5 A to handle the whole analyser. The rating can be reduced by 1 A for each RAM card that is omitted.

The five regulators are of the well-known 78xx type, but here rated at 2 A (S-type). This is because the current drain of the RAM cards is just about 1 A and it would be disturbing if the current limiting of the regulator would come into action regularly (low voltage).

The PCB for the supply is shown in Fig. 17. It has the same format as the bus board and the two may, therefore, if the enclosure allows, be fastened together with the aid of suitable spacers (track sides facing, of course). Such an arrangement would place the 5 V and 12 V connections of the boards close together.

Atari interface

Communication between an Atari and the logic analyser is via the hard-disk slot emerging at the rear of the computer via a D-type connector.

The present interface is not strictly a special hard-disk interface, but a DMA interface to which a maximum of eight external apparatuses may be connected in parallel. Addressing the apparatuses separately prevents any conflict between them. This means also that the hard disk may remain connected.

The circuit diagram of the interface is

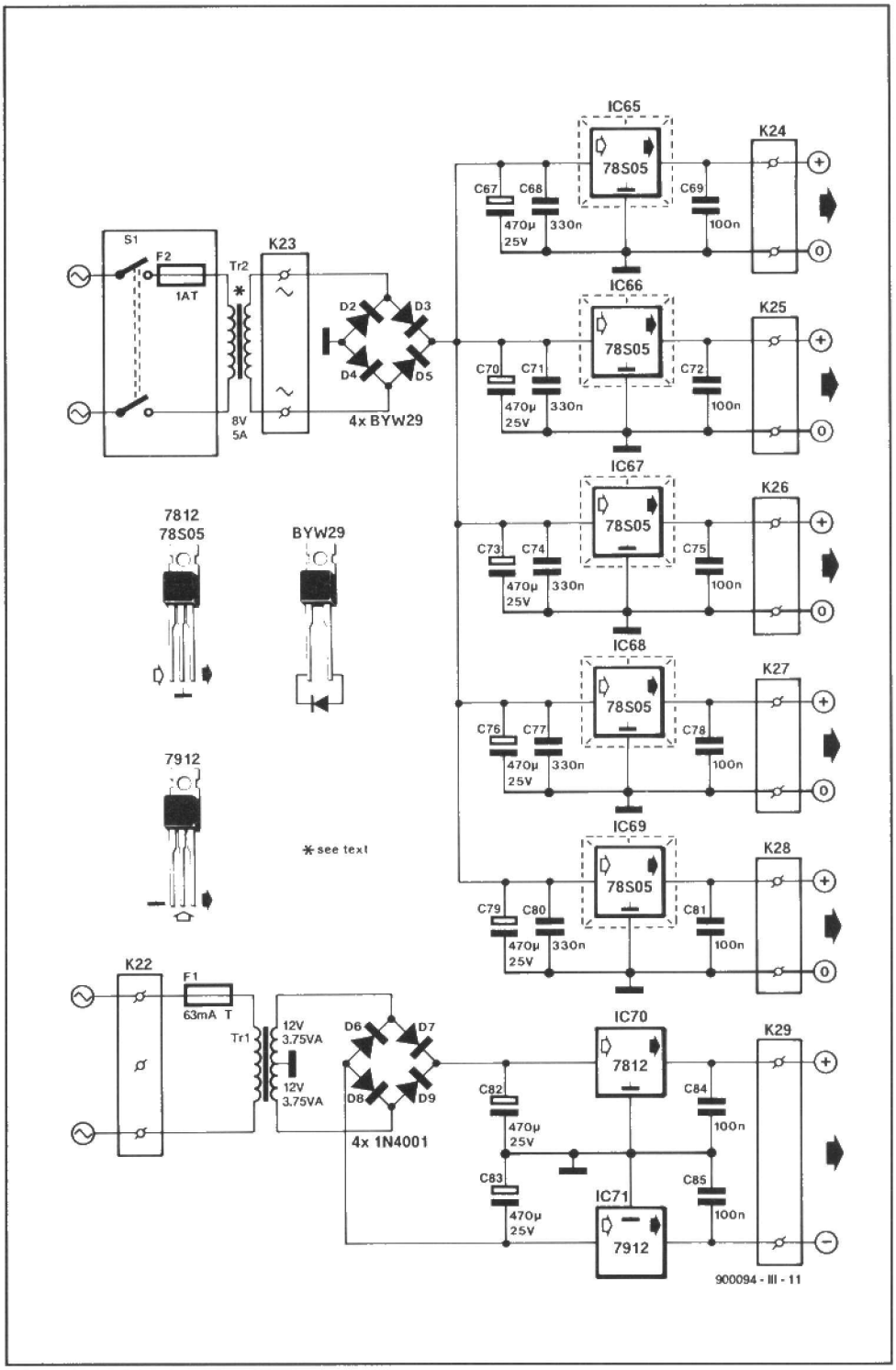


Fig. 16. Circuit diagram of the power supply; the section based on Tr1 is for use only if probes that accommodate input voltages up to ±12 V are to be used.

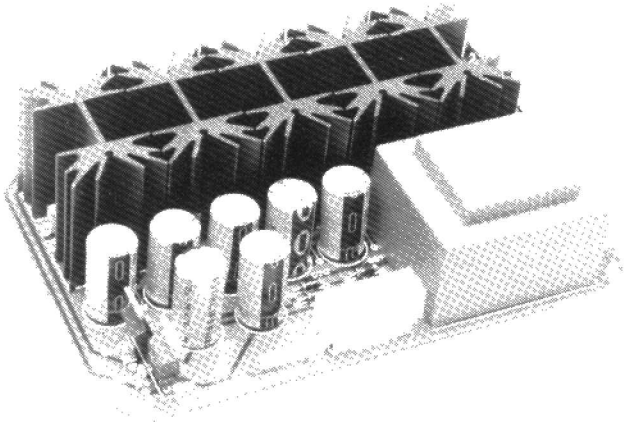
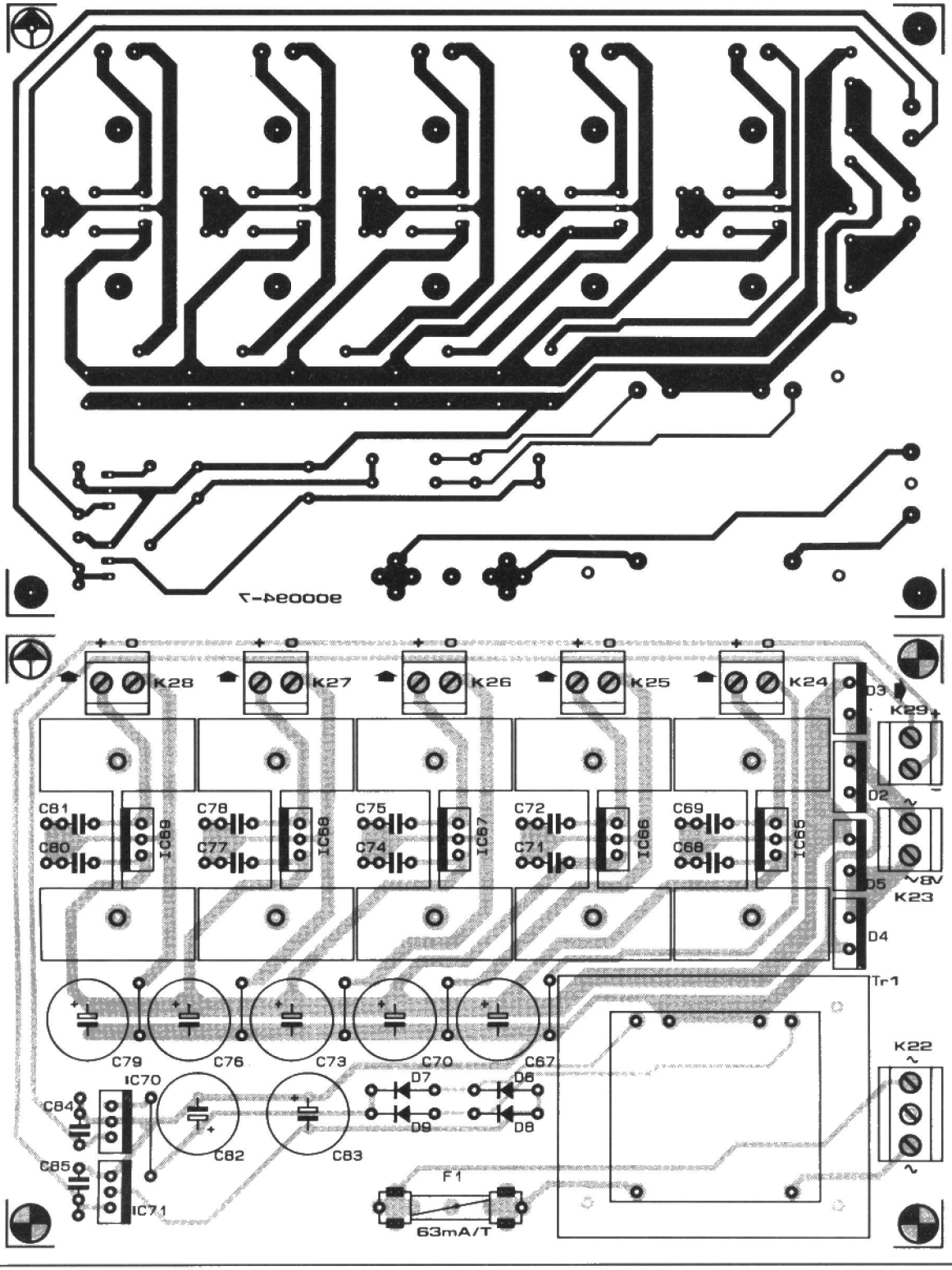


Fig. 17. Photograph of the completed power supply board.

Fig. 18. The printed-circuit board for the power supply has the same dimensions as the busboard. It has no provision for Tr2.



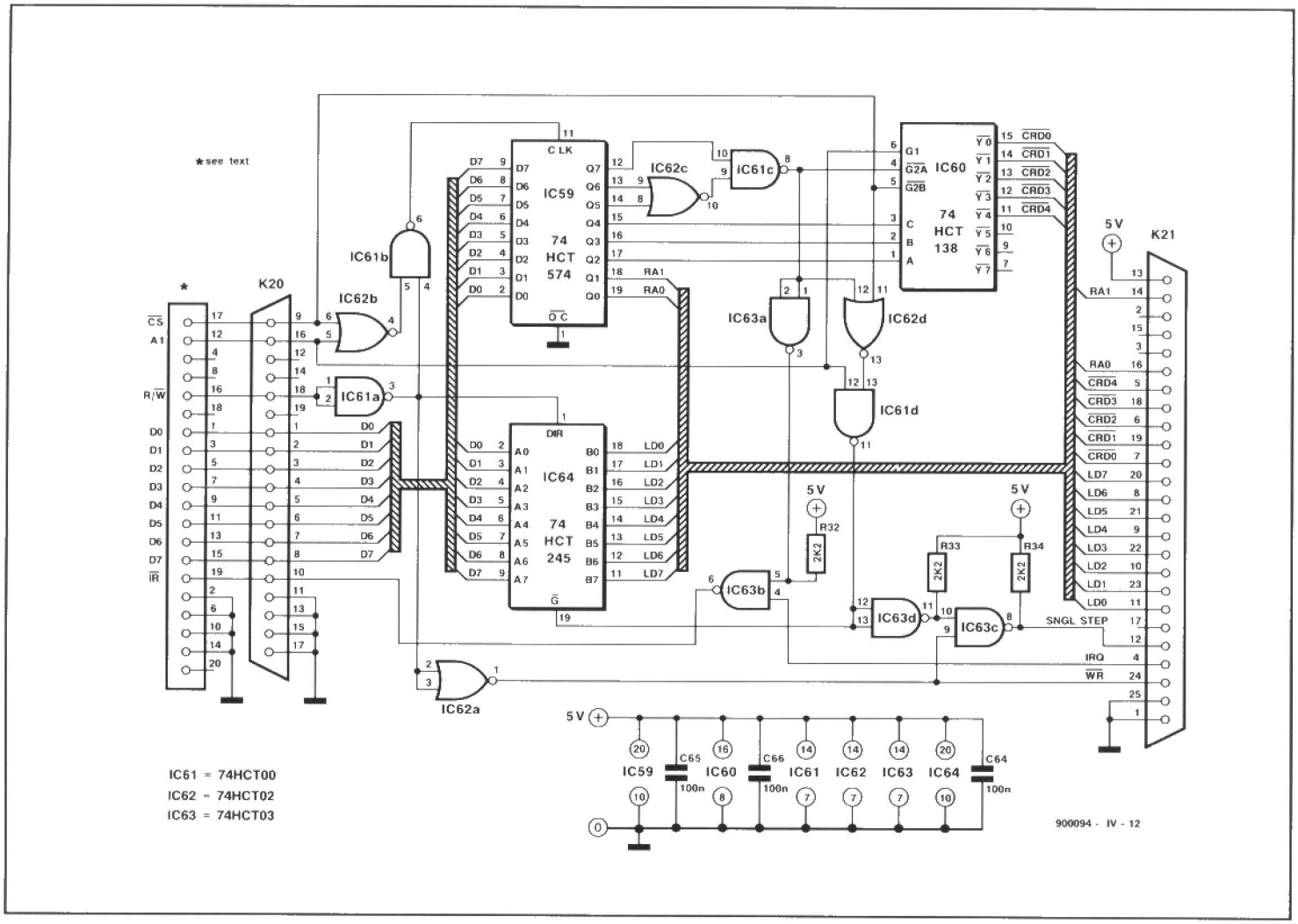


Fig. 19. Circuit diagram of the interface for Atari computers.

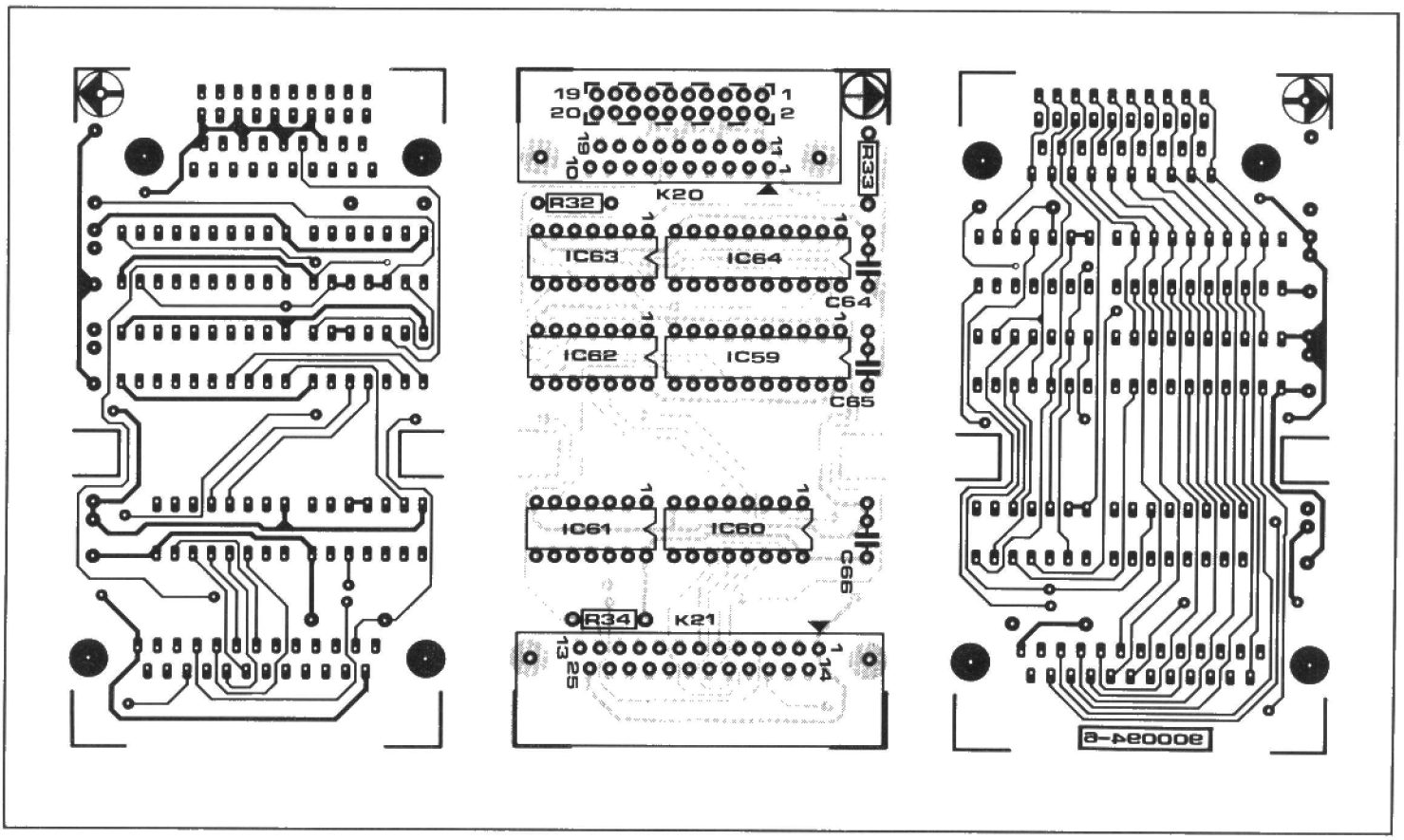


Fig. 20. The printed-circuit board for the Atari interface.

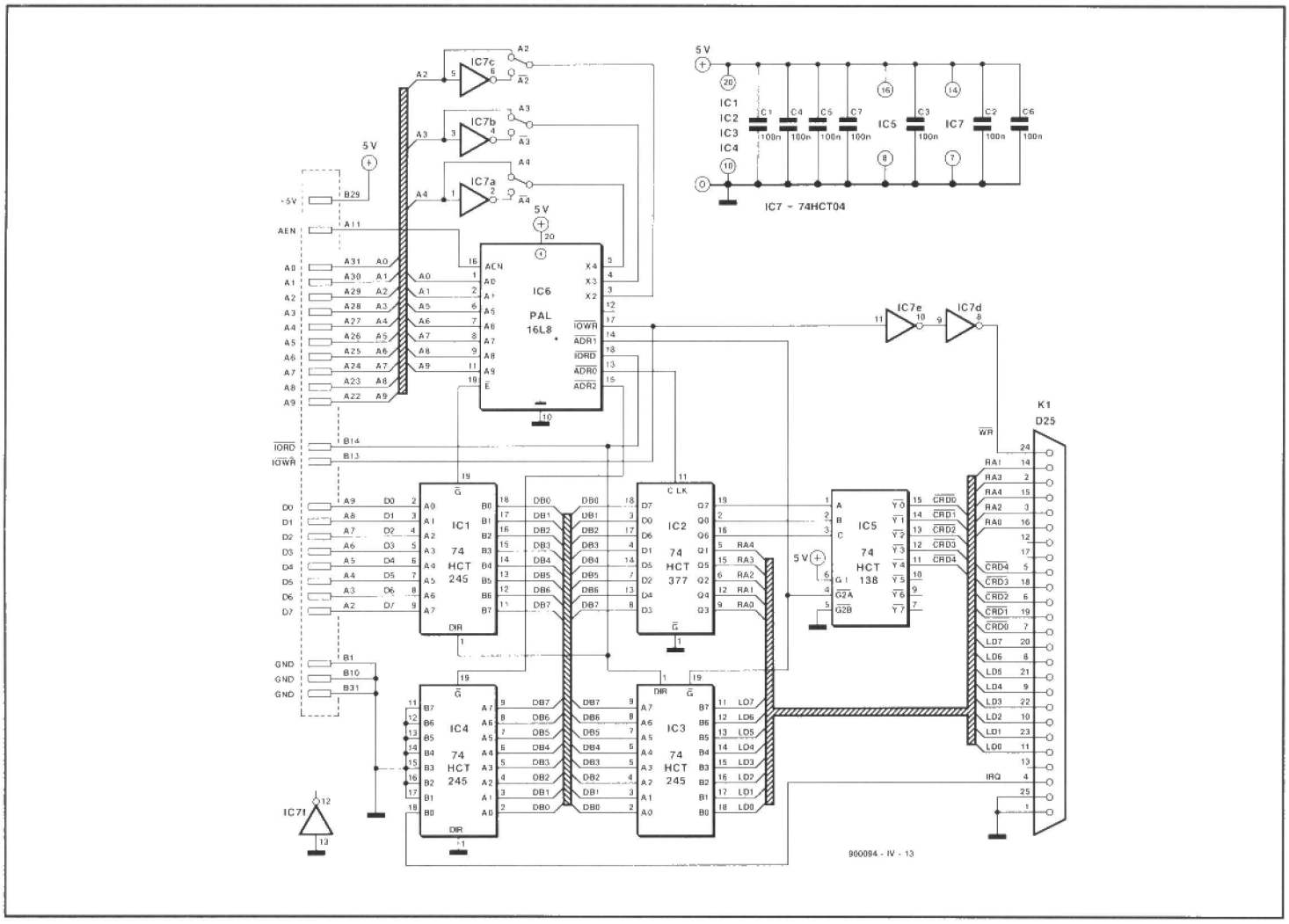


Fig. 21. Circuit diagram of the IBM interface.

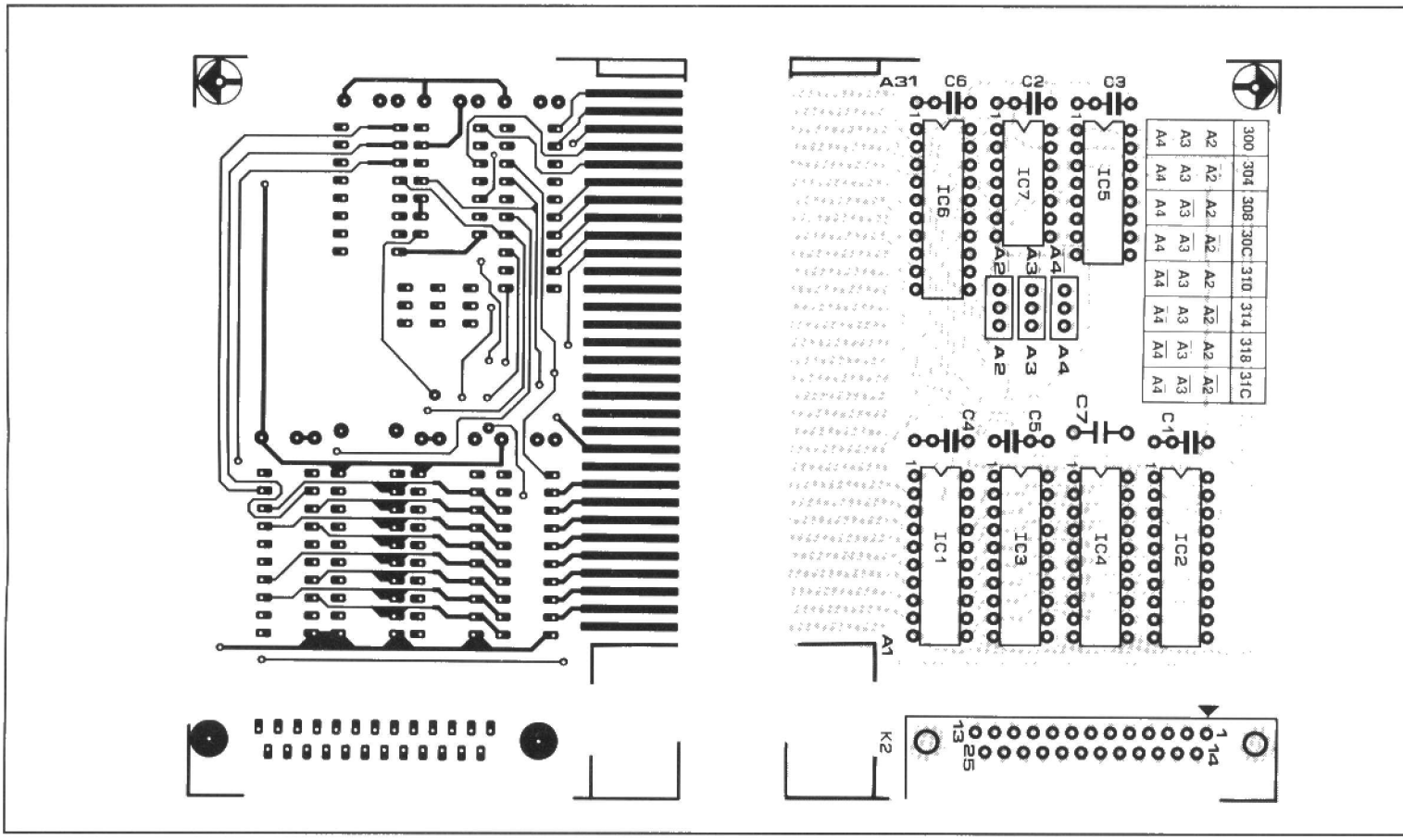


Fig. 22. The printed-circuit board for the IBM interface is designed as a slot-in card.

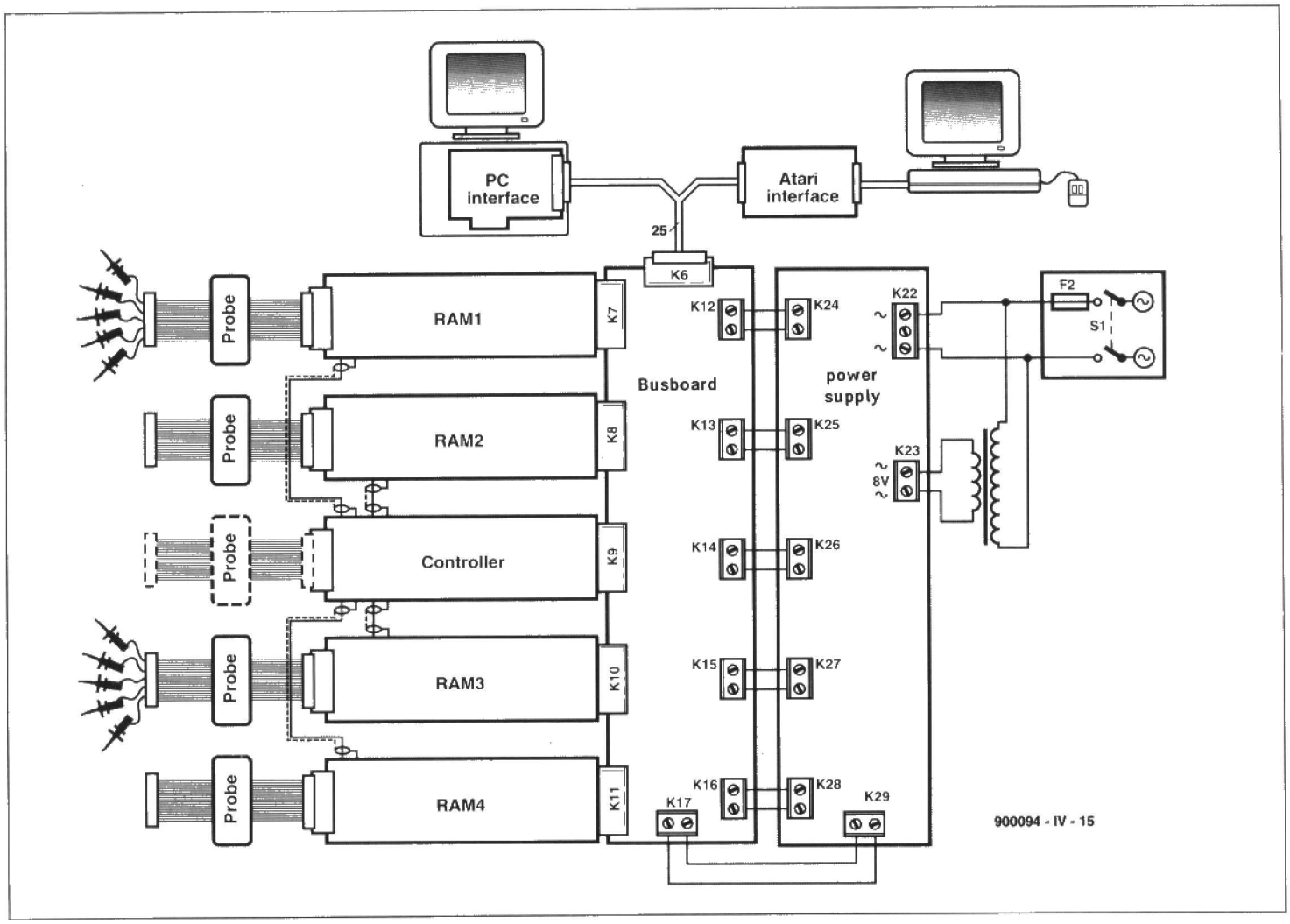
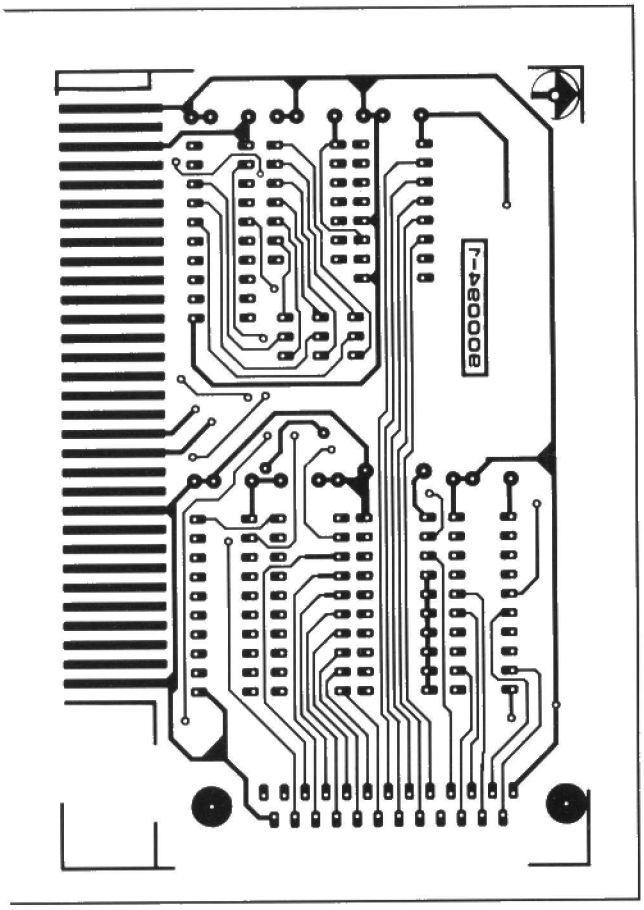


Fig. 23. Overview of the logic analyser and the wiring between the various boards.



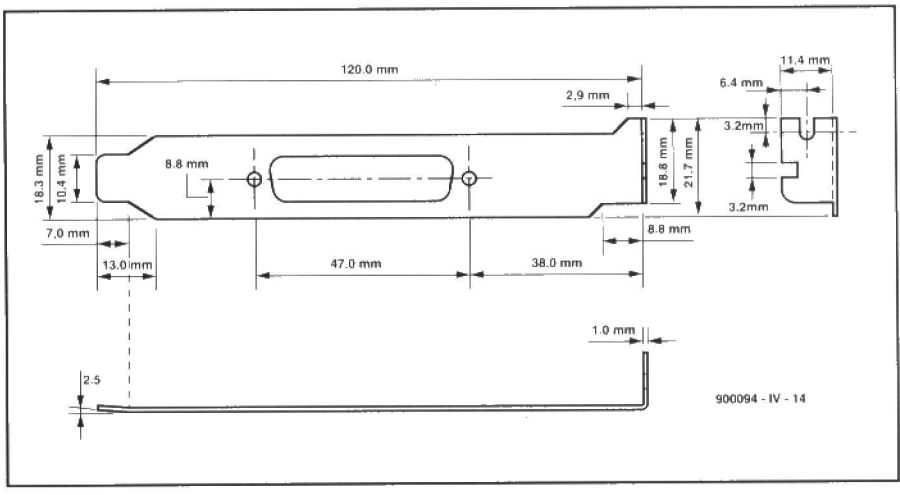


Fig. 24. The IBM interface print should be secured with a fixing plate as shown here.

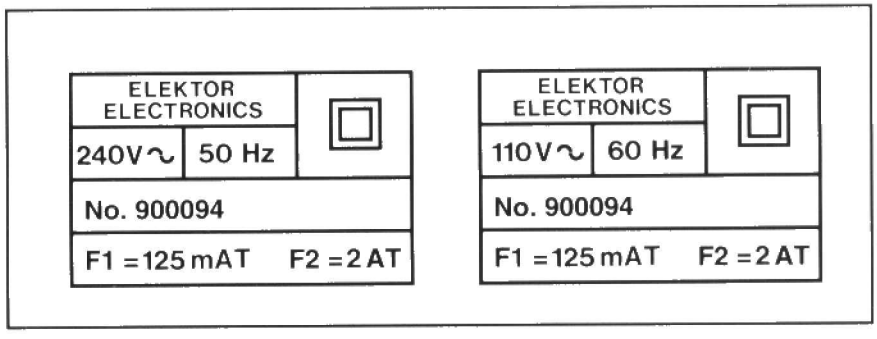


Fig. 25. Suggested labels for the rear panel of the logic analyser.

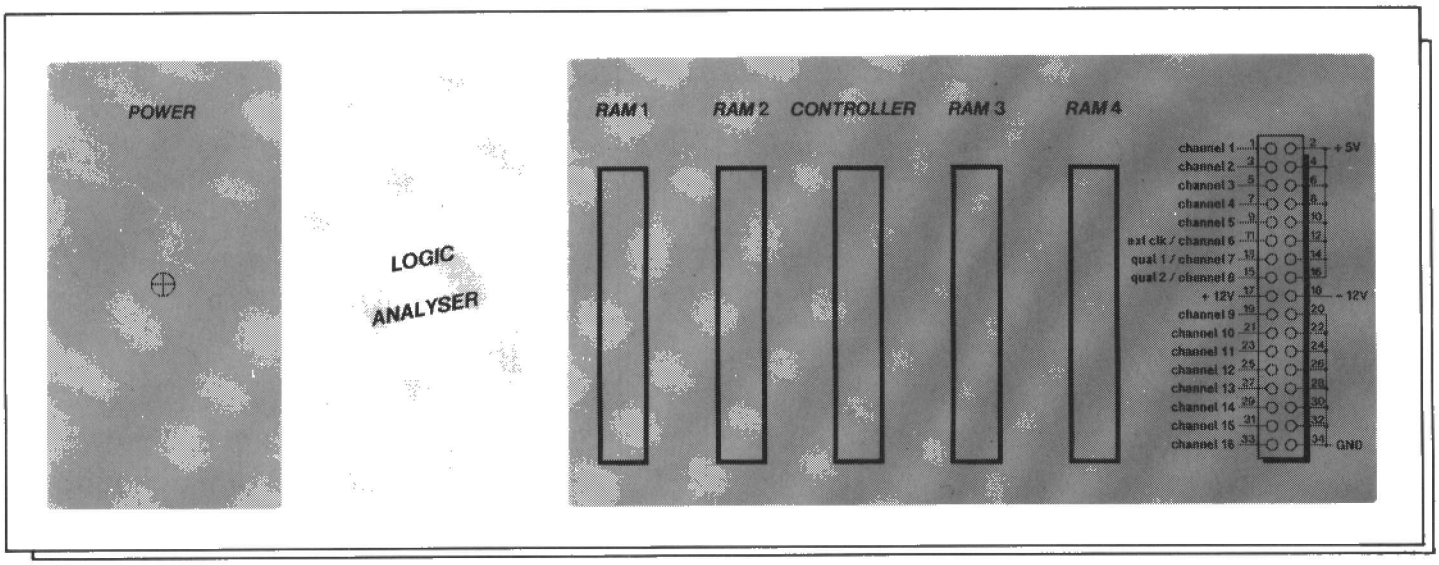


Fig. 26. The front panel for the logic analyser is available through our Readers Services.

PARTS LISTS

Power supply

Capacitors:
C67, C70, C73, C76, C79, C82, C83 = 470 µF, 25 V
C68, C71, C74, C77, C80 = 330 nF
C69, C72, C75, C78, C81, C84, C85 = 100 nF

Semiconductors:
D2–D5 = BYW29
D6–D9 = 1N4001
IC65–IC69 = 78S05
IC70 = 7812
IC71 = 7912

Miscellaneous:
K23–K29 = 2-way terminal block, 5-cm centre
K22 = 3-way terminal block, 5-cm centre
Tr1 = mains transformer, 12 V, 3.75 VA
Tr2 = mains transformer 8 V, 5 A
S1 = mains on/off switch with integral fuse holder
F1 = fuseholder and fuse, 63 mA, delayed action
F2 = fuse, 1 A, delayed action
Five heat sinks for IC65–IC69
PCB 900094-7

Atari interface

Resistors:
R32–R34 = 2.2 kΩ

Capacitors:
C64–C66 = 100 nF

Semiconductors:
IC59 = 74HCT574
IC60 = 74HCT138
IC61 = 74HCT00
IC62 = 74HCT02
IC63 = 74HCT03
IC64 = 74HCT245

Miscellanous:
K20 = 19-pole male D connector or 20-way box header (see text)
K21 = 25-pole female D connector for PCB mounting
PCB 900094-6

IBM interface

Capacitors:
C1–C7 = 100 nF

Semiconductors:
IC1, IC3, IC4 = 74HCT245
IC2 = 74HCT377
IC5 = 74HCT138
IC6 = PAL16L8 (Order No. 5973)
IC7 = 74HCT04

Miscellaneous:
K1 = 25-pole female D connector for PCB mounting
Fixing plate (see Fig. 22)
PCB 900094-1

shown in Fig. 19. The DMA interface can access two addresses in the circuit via line A1. The control register, IC_{59}, is at one of these addresses (A1 = 0). The address of the apparatus must be written in the three most significant bits of this register in order to actuate the analyser.

The logic analyser has address 4; whether that is stored in the control register is checked by gates IC_{61c} and IC_{62c}.

The output signal of IC_{61c} enables or disables the various inputs and outputs of the interface.

The remaining bits of the control register are used to address the various registers in the analyser proper: Q0 and Q1 provide the two address lines for the register, while Q2–Q4 control address decoder IC_{60}, which generates the five card-select signals.

When the interface is actuated by the four highest bits of the control register, data may be sent to and from the logic analyser via bidirectional buffer IC_{64}. The buffer is addressed when A1 is high. The direction of the data transport is determined by the read/write> line.

The single-step signal is produced by IC_{63c} and IC_{63d} from the strobe signal for the data bus and the WR> signal.

Atari interface board

The board for the Atari interface has been designed as a sort of adapter plug (see Fig. 20 and 27) that can be inserted at the rear of the computer. The PCB-type 19-way male D connector for this is, however, not easily available in many locations. There is, therefore, the possibility to use a box header (which is much more readily available) in the K20 position. Starting at pin 1, the wires in the cable

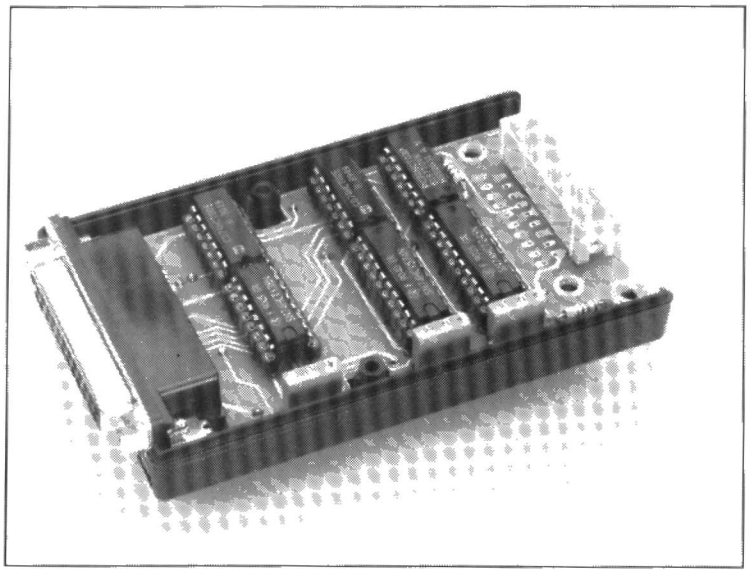


Fig. 27. Photograph of completed Atari interface board.

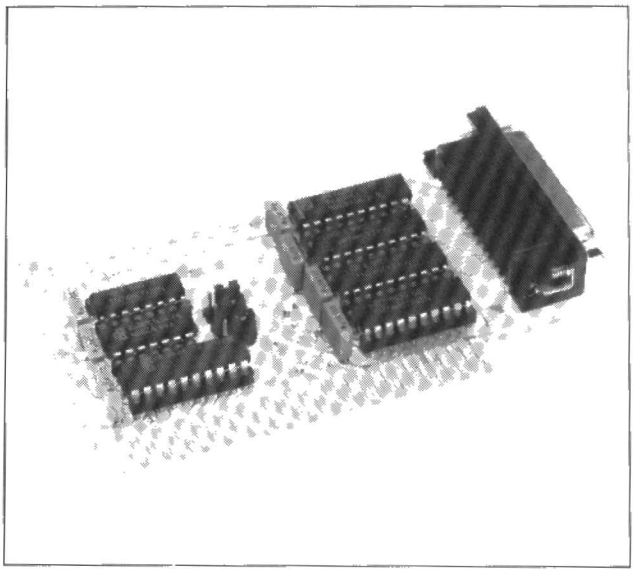


Fig. 28. Photograph of completed IBM interface board.

are soldered or crimped as follows: 1 to 1; 2 to 11; 3 to 2; 4 to 12; 5 to 3; and so on; only pin 20 of the box header is not used.

No such difficulties are envisaged with K_{21}. The cable between the interface and the logic analyser may be a standard computer accessory: 25-way with male and female connectors. It should, however, not be longer than one metre.

IBM interface

The interface for IBM XT and AT computers consists of not much more than a number of digital inputs and outputs—see Fig. 21. The data bus for the computer is buffered by IC_1. This is not necessary for the address lines of the computer, since most lines are connected to only one input. There are, nevertheless, three address lines that, depending on the position of the jumpers near IC_6, are loaded with up to two inputs. Circuit IC_6 is the address decoder of the interface.

The basic address of the card may be arranged in steps of four addresses from 300_{hex} to $31C_{hex}$ with the aid of jumpers and inverters in lines A2–A4.

Four addresses emanate from the address decoder (a PAL): an enable signal for the data bus buffer (E>) and three select signals for controlling the three individual addresses on the interface card: ADR0–ADR2.

The address register is found at basic address +0. The address with which a card and a register are addressed on that card is written in the address register.

The data register is found at basic address +1, via which data are written to, or read from, the logic analyser. Simultaneous with the reading or writing, card select decoder IC_5 is enabled via the ADR1 line to ensure that the cards of the analyser are connected to the bus only when this really necessary.

The IRQ signal from the analyser enters via basic address +2 on the interface card. This is processed as data, and not as an interrupt.

IBM interface board

The dimensions of the PCB for the IBM interface are determined solely by those of the two connectors—see Fig. 22 and 28. Since the electronics do not need much space, it has been possible to include a table on the board that indicates what jumpers are required to place a certain basic address for the card.

To prevent the card being pulled from the slot by the connecting cable, it is essential that the board is provided with a fixing plate with which it can be fastened securely on to the computer. Such a plate can be made as shown in Fig. 24.

For the connection between the interface and the computer the same sort of cable as for the Atari may be used.

Overview

An overview of the logic analyser and all that may go with it is shown in Fig. 23.

The control card is always connected to the centre connector of the bus board to ensure that when several RAM cards are used, the connections between these cards and the control card remain as short as feasible.

Before the RAM cards are built in, a 10 kΩ resistor must be soldered at the track side between pins 11 and 16 of IC_{29}. This resistor suppresses any reflections that may occur at that end of the clock line to the shift registers.

There is not much wiring in the analyser because most connections are contained on the bus board. What wiring there is comes mainly from the power supply. ■

10K R5 ACROSS SOCKET B5
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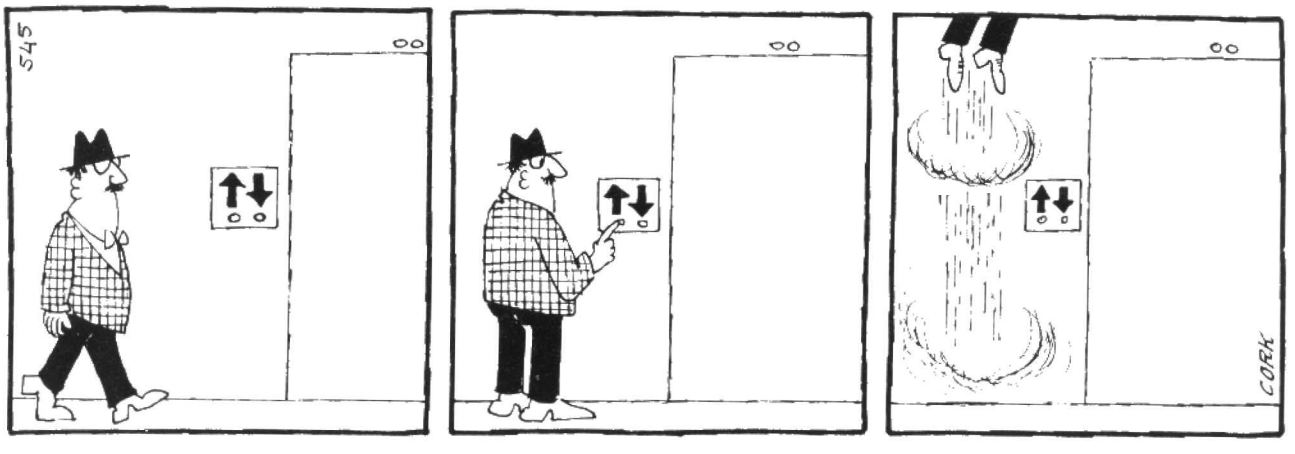


VIDEO A-D/D-A CONVERTER

PART 2: A 30-MHz VIDEO ADC/DAC DEVELOPMENT BOARD

Following last month's introduction into the basic operation of the two main integrated circuits in the design, the TDA8708 and the TDA8702, this second and last instalment focuses on the more practical side of things. Are you triggered? Here is a high-speed video A-D/D-A converter board aimed at helping you on the way with your own video experiments.

P. Godon (Philips Components, Paris)

Continued from the May 1991 issue

The block diagram of the development board, Fig. 8, shows the two converter ICs surrounded by quite a few sockets, switches and connectors. The switches, K1 through K9, are actually jumpers that allow different modes of operation to be selected. The BNC sockets, K10 through K17, are the analogue

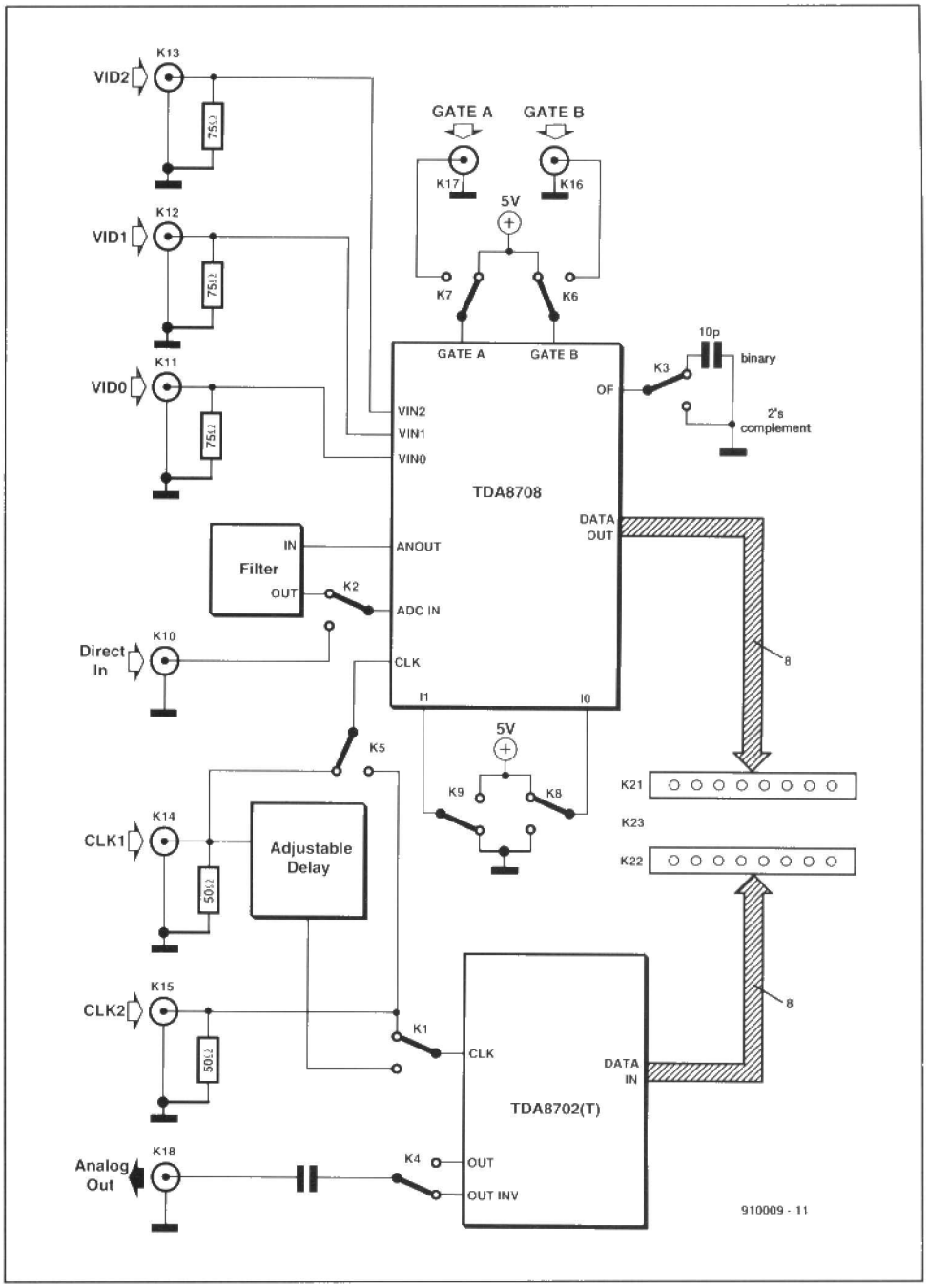


Fig. 8. Block diagram of the video processor card. Most of the switches shown here are wire jumpers to select different modes of operation.

Table 8. Connector overview

Connector	Type	Function
K1	jumper	Clock 2 / delayed Clock 1
K2	jumper	Video input / direct input
K3	jumper	ADC output: binary or 2's complement
K4	jumper	DAC output: true or inverted
K5	jumper	Clock 1 / Clock 2
K6	jumper	Gate B active / disabled (+5 V)
K7	jumper	Gate A active / disabled (+5 V)
K8	jumper	Video input selection: Bit 0=H / Bit 0=L
K9	jumper	Video input selection: Bit 1=L / Bit 0=H
K10	BNC socket	ADC direct input
K11	BNC socket	ADC input 0
K12	BNC socket	ADC input 1

Connector	Type	Function
K13	BNC socket	ADC input 2
K14	BNC socket	Clock input 1
K15	BNC socket	Clock input 2
K16	BNC socket	Mode gate B
K17	BNC socket	Mode gate A
K18	BNC socket	DAC analogue output
K19	PCB pin	Clock delay
K20	PCB header	Supply voltages
K21	PCB header	ADC output
K22	PCB header	DAC input
K23	32-way DIN	combined ADC output and DAC input

video inputs and the digital control inputs. The analogue output signal of the DAC is available on socket K18. The board is linked to a computer or microprocessor system via connectors K21 and K22, or K23. All digital inputs and outputs of the board are TTL compatible.

The development board is connected to analogue and digital 5-V power supplies via K20. Two separate power supplies are required to ensure the best possible decoupling of the analogue and digital sections.

The 'adjustable delay' block is formed by an integrated circuit that has not been discussed last month. This IC, a Type 1505-5B from Data Delay Devices, contains a stepped delay line. The signal applied to the CLK1 input of the board, K14, can be delayed in steps of 1 ns to a maximum of 5 ns. The delay line has a d.c. resistance of 0.7 Ω and an impedance of about 100 Ω.

Finally, the resistors shown in the block diagram ensure that video sources are terminated in 75 Ω, and the clock inputs in 50 Ω.

The development circuit

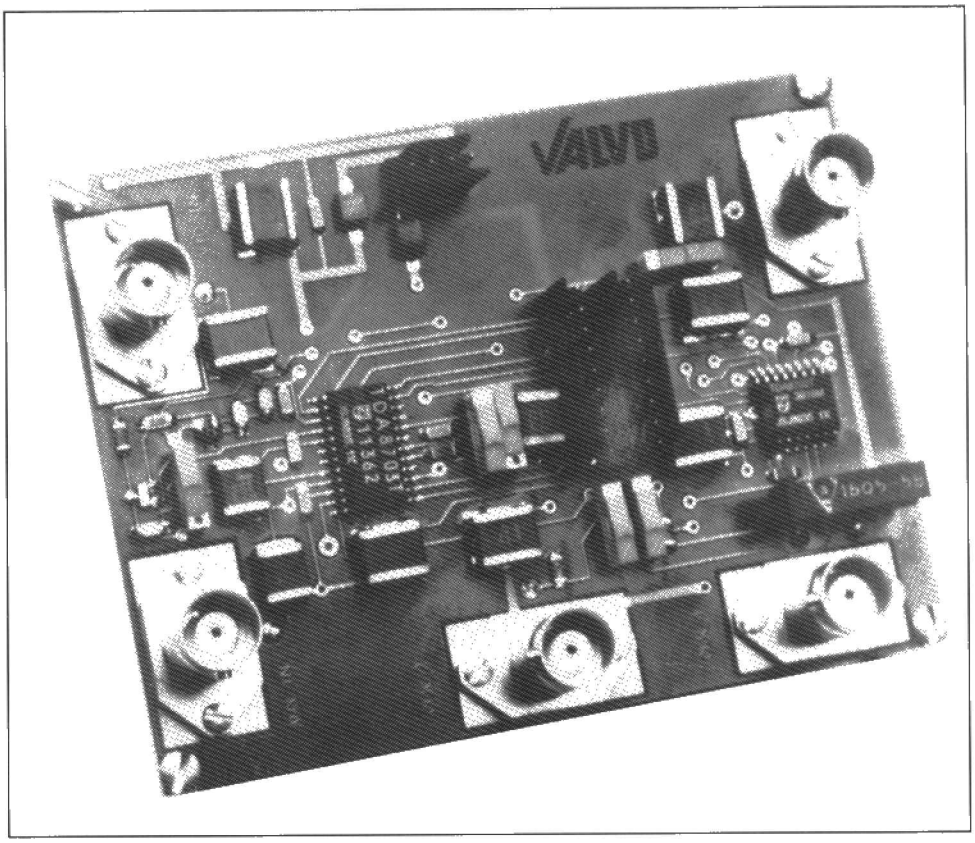
The circuit diagram of the video A-D/D-A card is given in Fig. 10. As discussed last month, the TDA8708 stores the current analogue value at the first leading edge of the clock signal, after the 1.5-V threshold is exceeded. You will also recall that the digital equivalent of the analogue value appears at the output after a delay, T_d, of 8 to 20 ns. At the next trailing edge of the clock signal, the DAC copies the digital information, and supplies the corresponding analogue value after the conversion delay, t_d, of 3 ns. Hence, the video input signal is subject to a total delay, T_v, of

$$T_v = T_d + \tfrac{1}{2}f + t_d$$

At relatively high clock frequencies, say, 30 MHz, it may happen that the minimum required delay time between the A-to-D and D-to-A conversions is not available. The DAC requires that the input data remain stable for at least 0.3 ns. Since the time between the leading and the trailing edge is only 17 ns for a 30-MHz clock signal, it is readily seen that the DAC may have trouble loading stable data when the required delay, T_d, is yet to be subtracted. This potential problem is eliminated by the previously mentioned delay line, IC3, which delays the trailing edge of the clock 1 to 6 ns, depending on the selected 'tap' (jumper K19). This compensation ensures the correct operation of the conversion processes when relatively high clock speeds are used. The diagram in Fig. 9 shows the combined timing of the ADC and the DAC, along with the data setup times and associated delays.

Construction

In view of the speed of the signals involved, the video A-D/D-A circuit is best built on a printed-circuit board of the design shown in Fig. 11. The board is double-sided, but not



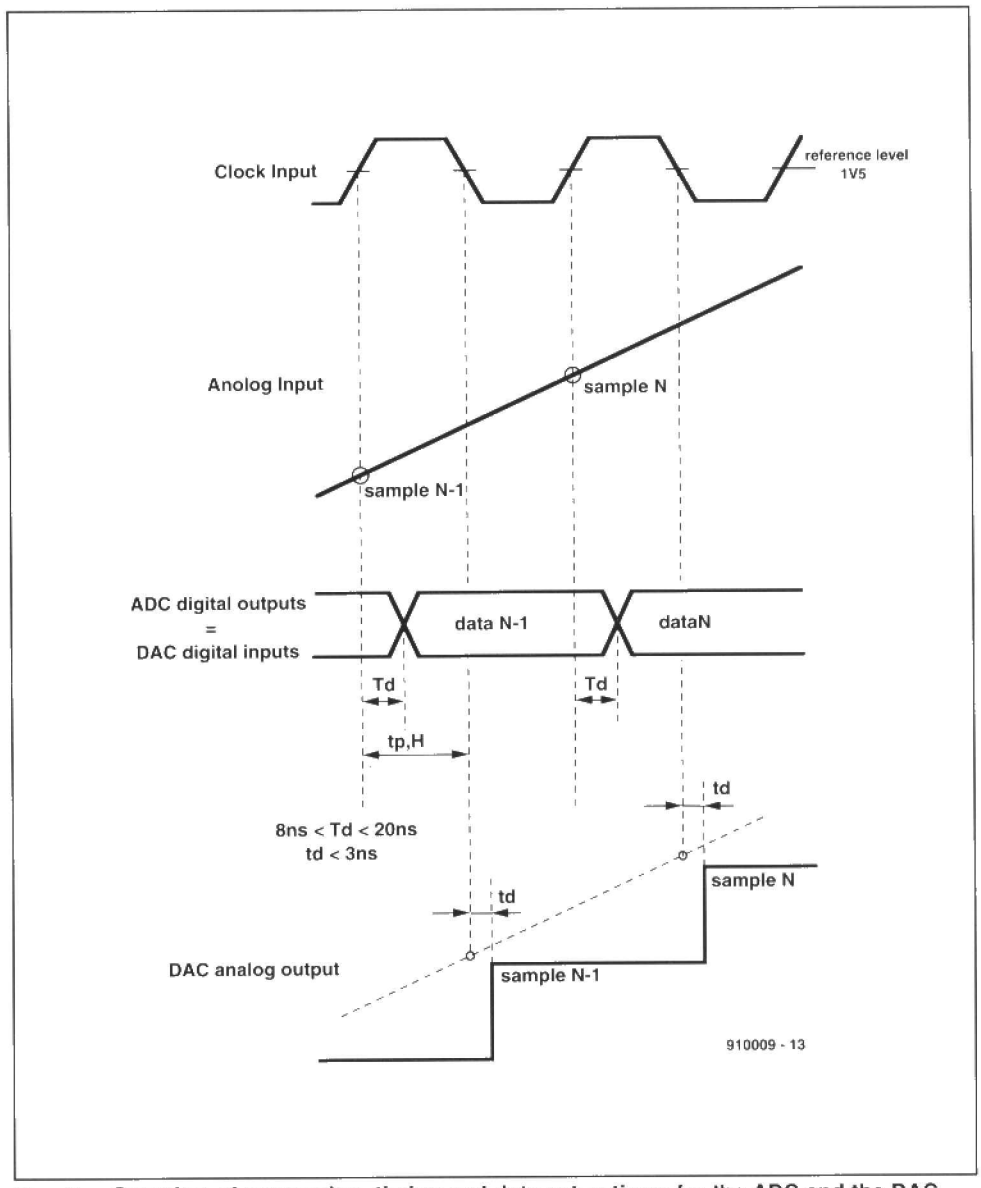


Fig. 9. Overview of conversion timing and data setup times for the ADC and the DAC.

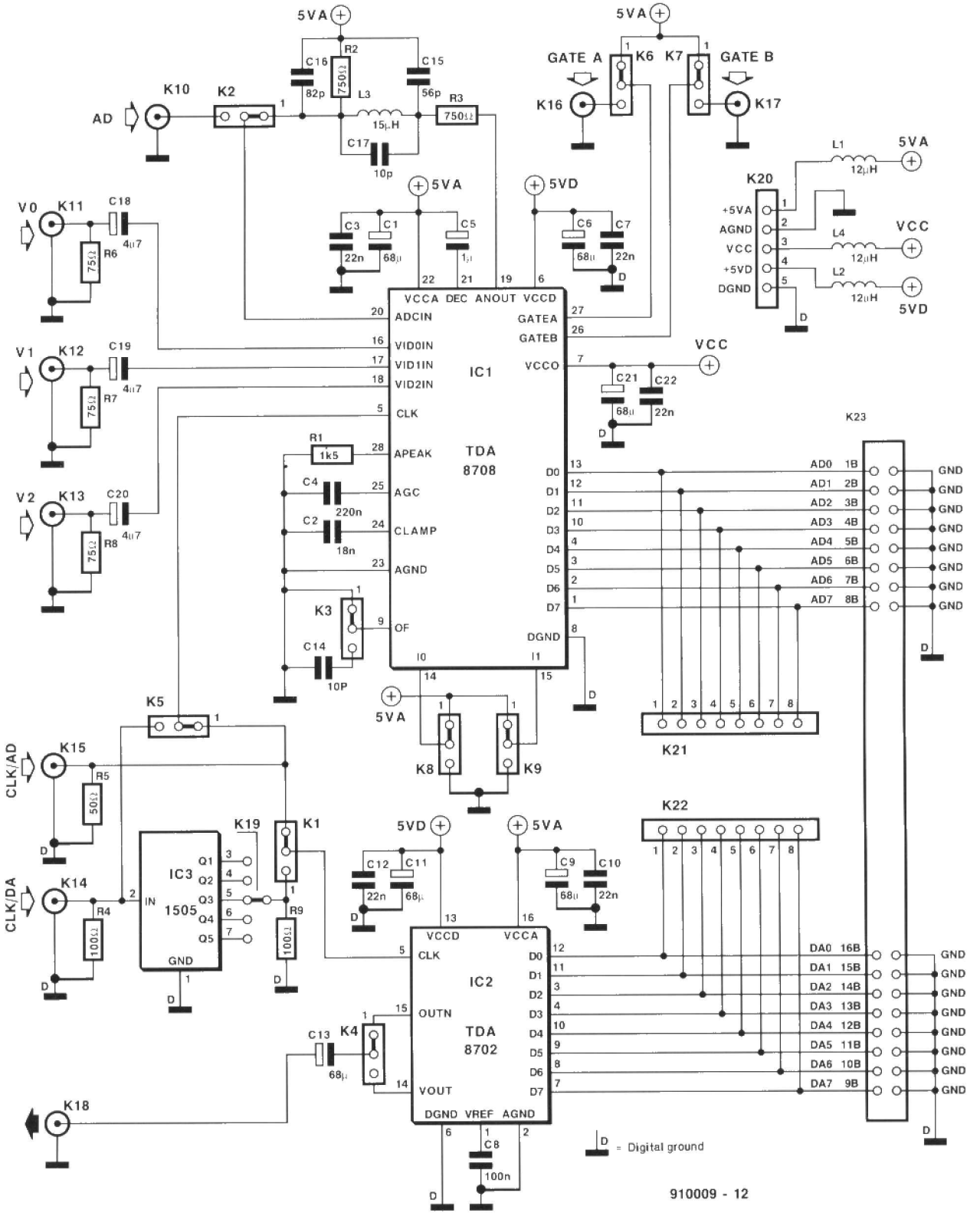


Fig. 10. Circuit diagram of the ADC/DAC converter card. You have the digitized video signal available at a resolution of 8 bits between connectors K21 and K22. A separate connector, K23, allows the card to be connected to a computer bus.

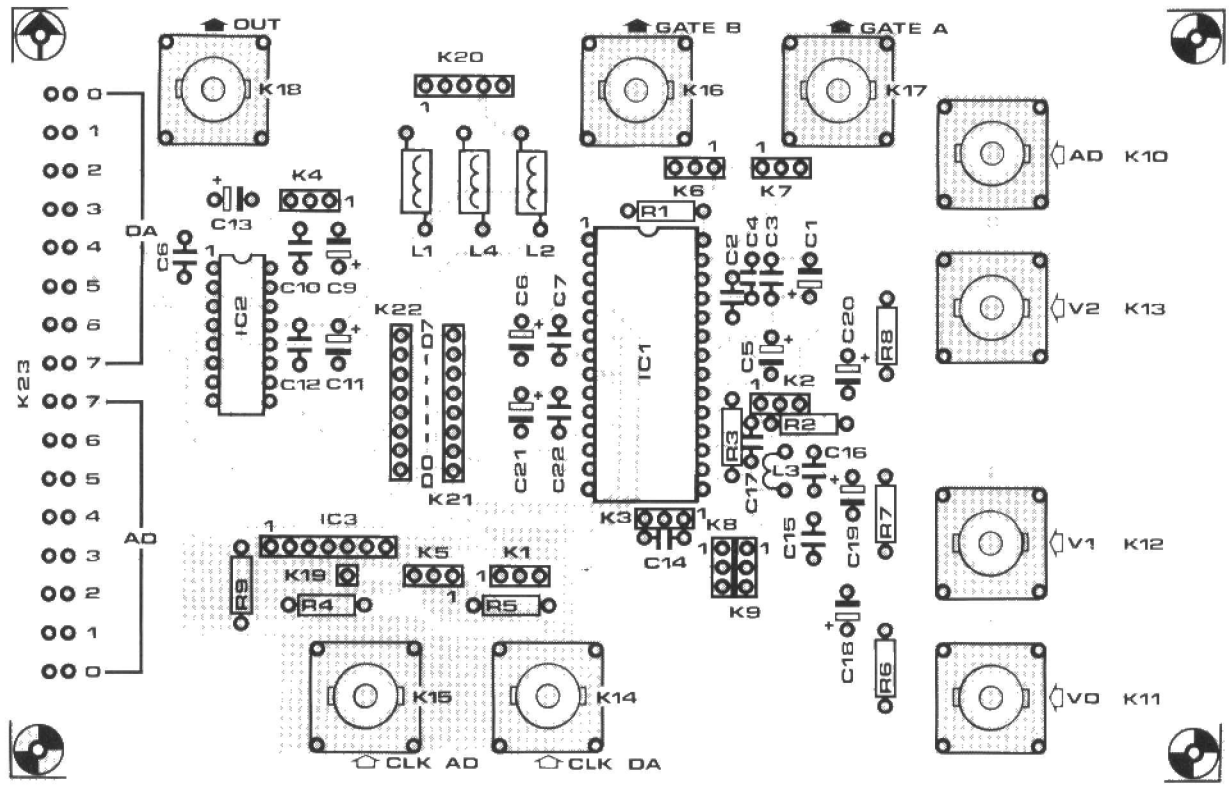


Fig. 11a. Component mounting plan of the double-sided printed circuit board. Note that the board is designed for PCB-mount BNC sockets.

through-plated. Its design allows BNC sockets to be fitted without coaxial cables, which reduces parasitic capacitance to a minimum.

Most of the PCB headers and jumper blocks on the board can be made from single-row and double-row pin headers, which are available in strips of 36 and 72 pins with a spacing of 0.1 inch. Headers K21 and K22, for instance, are 8-pin pieces cut from a larger strip.

Connector K23 is a 32-way angled type to DIN41612. It allows the digital data inputs of the DAC, and the digital outputs of the ADC, to be connected to a microprocessor system bus. For a straight link between the ADC and the DAC, interconnect the corresponding pins on K21 and K22. Finally, note that although an SMA (surface-mount assembly) version of the development board is shown in Fig. 11, all components on the board shown in Fig. 10 have standard sizes. ■

COMPONENTS LIST

Resistors:

1	1kΩ5	R1
2	750Ω	R2;R3
2	100Ω	R4;R9
4	75Ω	R5 - R8

Capacitors:

6	68µF 6V3	C21
1	18nF	C2
5	22nF	C3;C7;C10; C12;C22
1	220nF	C4
1	1µF 10V	C5
1	100nF	C8
2	10pF	C14;C17
1	56pF	C15
1	82pF	C16
3	4µF7 10V	C18;C19;C20

Inductors:

3	12µH	L1;L2;L4
1	15µH	L3

Miscellaneous:

1	TDA8708	IC1
1	TDA8702	IC2
1	1505-5b *	IC3
9	3-pin PCB header	K1 - K9
9	PCB-mount BNC socket	K10 - K18
1	solder pin	K19
1	5-pin PCB header	K20
2	8-pin PCB header	K21;K22
1	32-way angled connector to DIN41612	K23

0.1-inch jumpers as required

* UK distributor: BFI Ibexsa Electronics • Burnt Ash Road • Quarrywood Estate • Aylesford • Kent ME20 7NA. Tel. (0622 882467), Fax (0622) 882469.

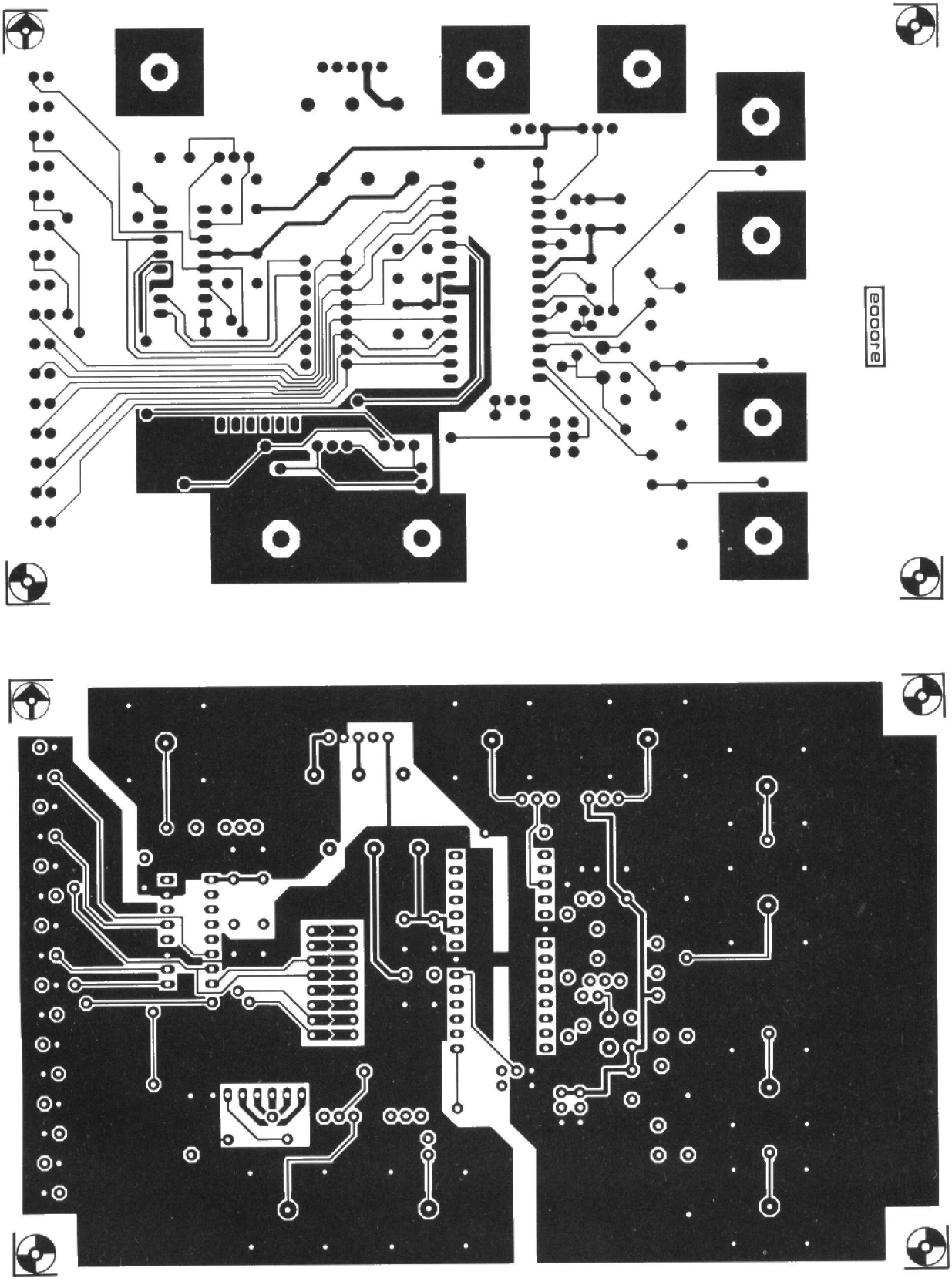


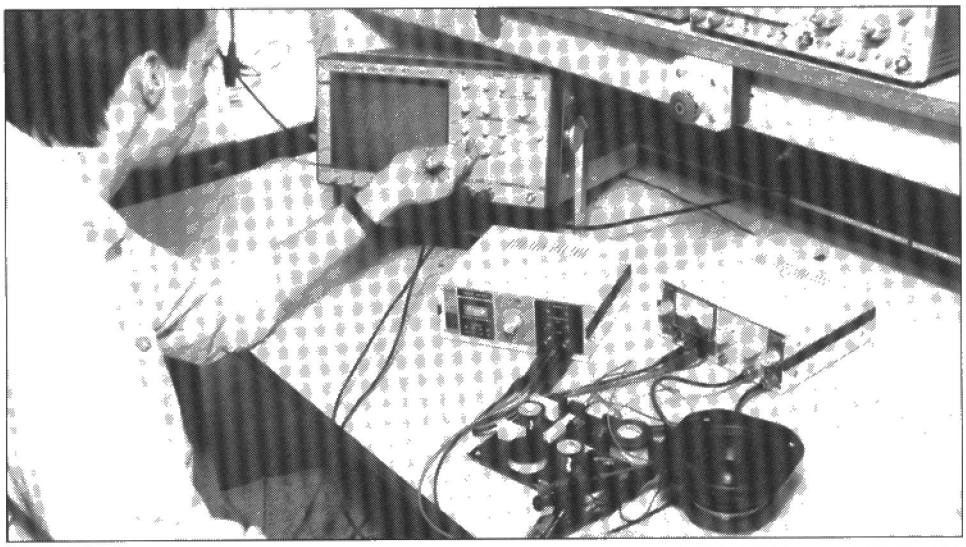
Fig. 11b. Solder side (above) and component side (below) of the PCB for the video ADC/DAC card.

DIGITAL PHASE METER

FRONT COVER PROJECT

by R. Lucassen

Phase meters are rare instruments, even in the laboratory or workshop of audio and hi-fi engineers and enthusiasts. Perhaps that is because until the advent of reliable digital techniques it was fairly difficult to design an accurate direct-reading phase meter. In one commercial catalogue published in the 1970s, a phase meter is advertised as having "an accuracy of about 3 degrees from 10 Hz to 30 kHz". Clearly, for modern audio equipment, that is no longer acceptable. Another reason may be that a phase meter is a fairly specialized instrument: many engineers and technicians measure phase shift with the aid of Lissajous figures (which do not give very accurate results either). The phase meter presented in this article is accurate to within 0.5° over the frequency range 10 Hz to 20 kHz.



THE PHASE shift between two electrical signals is of great importance in most branches of electronic engineering, but more particularly in audio engineering. In all circuits containing capacitors or inductors or both, frequency-dependent phase shifts will occur and these will affect the wanted operation of many circuits. There are, of course, circuits, such as filters, where phase shift is one of the design parameters.

The basic design of the phase meter may be gleaned from the block diagram in Fig. 1. Note, however, that, for the sake of simplicity, an analogue meter has been substituted for the LED display with which the instrument is actually equipped.

The analogue signals presented to the display section are digitized before they are processed. Since alternating signals are involved, this is quite simple: the positive part of the signals is converted to a logic low (0) and the negative part to a logic high (1). The timing diagram in Fig. 2 shows the analogue input signals (A and B) together with their digitized variants (A' and B'). The use of the digitized signals as the clock for a bistable (US: flip-flop) ensures a perfectly symmetrical (i.e., duty factor is 50%) digital output signal at a frequency equal to half that of the input signal. This guarantees that differing lengths of positive and negative half periods, noise and other spurious signals have no effect on the accuracy of the measurements.

The time difference between the leading edges of the signals emanating from the bistables is a measure of the phase shift between the two input signals. The output of the XOR gate is high during this time difference. The ratio of the width of the logic high signal at the output of the XOR gate to that of the output signal of bistable FF_1 gives the phase shift, which only has to be converted into degrees.

The width of the output pulse of the XOR

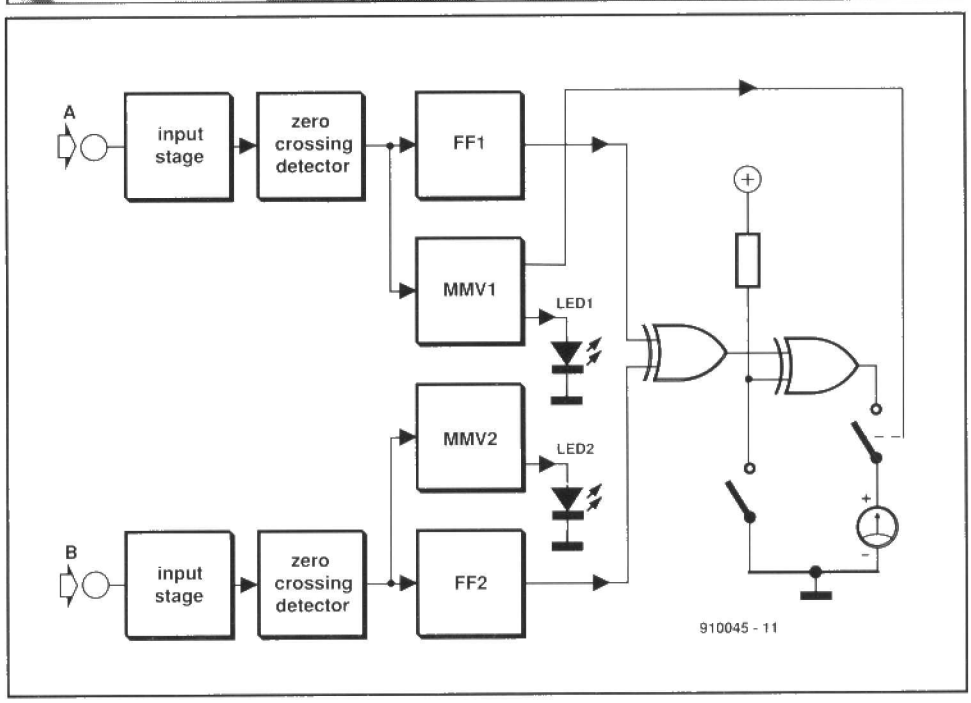


Fig. 1. Block diagram of the digital phase meter.

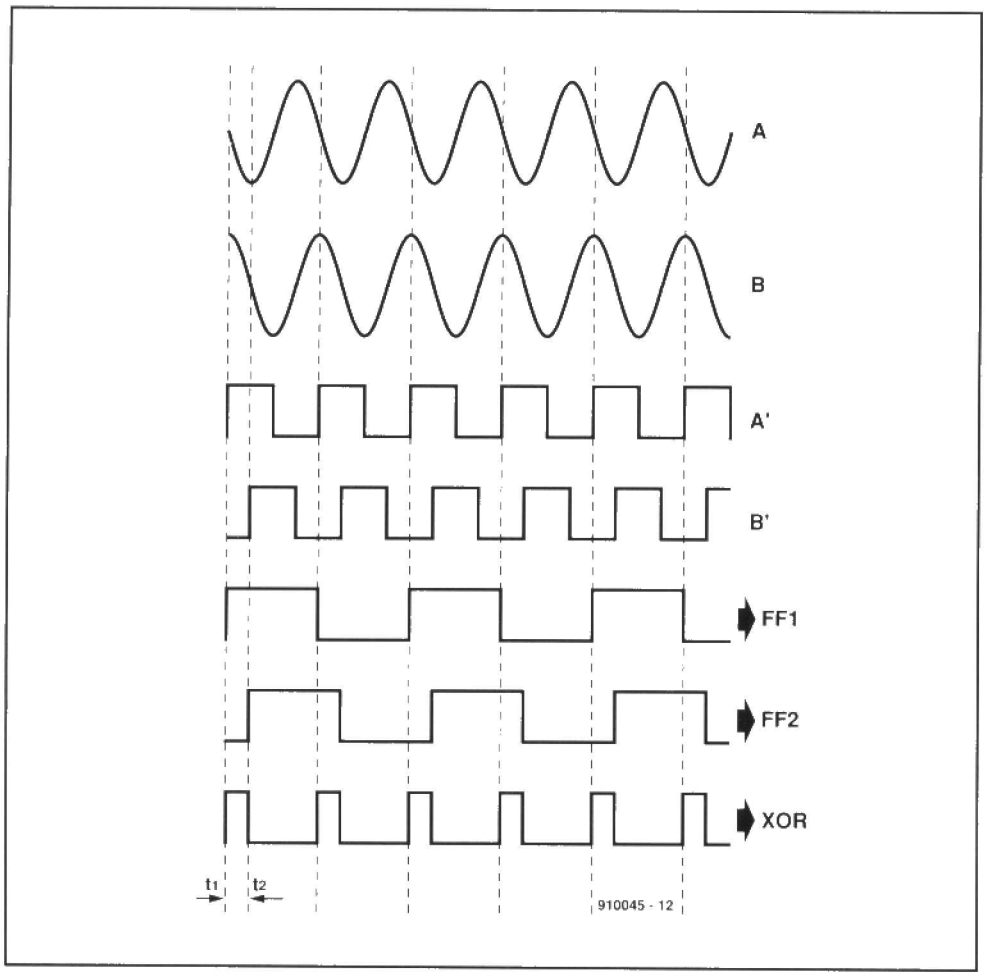


Fig. 2. Timing diagram of the analogue-to-digital conversion section.

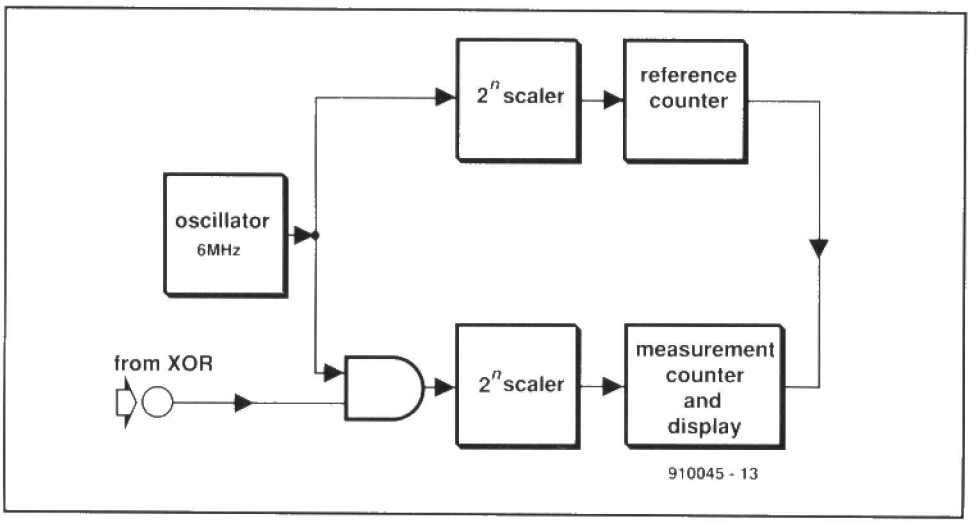


Fig. 3. Block diagram of the digital measuring section.

gate indicates at all times by how much signal B lags signal A. Therefore, the pulse represents a phase difference of 0–360°. Since it may also be of interest to measure the lag of signal A with respect to signal B, there is a second XOR gate whose output may be inverted.

Monostables MMV_1 and MMV_2 indicate by LEDs that usable signals, that is, signals whose phase difference is to be measured, exist at the associated inputs. Furthermore, the output of MMV_1 is used to actuate the meter. If only signal A is present, the meter must remain stably in the centre position. If it does not, the input signal is unstable and, therefore, not suitable for measurements.

Since the width of the pulse at the output of the XOR gate is a measure of the phase shift, it would seem that a simple analogue interface in the form of an integrator would be sufficient for driving a moving meter. That would, however, present certain difficulties, such as a strong dependence on temperature and the fact that to obtain a stable meter deflection a high integration constant would have to be used. That would make the measurement very slow and the instrument inconvenient to use.

A digital meter was therefore chosen, which can accurately indicate any phase difference between 0° and 360° with a resolution of 1°. The diagram in Fig. 3 shows how this meter operates.

A central clock frequency of 6 MHz is used, which is applied continually to one branch of the circuit, and to the other branch only when the output of the XOR gate of the phase comparator is high. In both branches, the clock pulses are divided by 2^n before they are applied to the respective stage. Factor n is set manually. Note that since division takes place after the AND gate, this gate has no effect on the accuracy of the measurement.

As soon as the content of the reference counter has reached a value of 3,600, one output of the counter goes high to indicate that the measurement is complete and that $3{,}600 / 2^n$ pulses were processed during it.

At the instant the reference counter has counted 3,600 pulses, the display memory is prompted to take over the contents of the reference counter. The display will then show the number of counted pulses, that is, when the phase shift is 0°, no pulses were counted; if the phase shift is 360°, 3,600 pulses were counted. The last digit of the number of pulses is omitted to make the display read the number of degrees.

Note that the accuracy of the measurement depends on the ratio of the measuring time to the frequency of the reference signal. The measurand is therefore sampled at a frequency of 6 MHz. Even at the highest signal frequency of 20 kHz, the error introduced by this is negligible

Furthermore, the design of the instrument arranges that counting always starts at the beginning of a period. Therefore, it is never known how much of the last period is measured and steps must consequently be taken to ensure that the last period has negligible influence on the measurement. This is done by taking many periods per measurement. For instance, a measurement over 10 periods has a possible error of 10%, whereas over 200 periods the error would be only 0.5%. Because of that, the instrument contains a counter (in the error indicating circuit) that monitors over how many signal periods a measurement. was spread.

Circuit description

The instrument is constructed on three printed-circuit boards; the associated circuits are shown in Fig. 4, 5 and 6.

Figure 4 is the circuit diagram for the motherboard. The power supply is a straightforward, conventional type with a bridge rectifier and two integrated regulators.

The buffered and possibly attenuated (–20 dB) signal is applied to terminals A and B. Input A is used as the reference signal and for actuating the metering section.

The incoming analogue signal is converted into a digital signal in IC_{12} (channel A) and IC_{14} (channel B). The offset of these

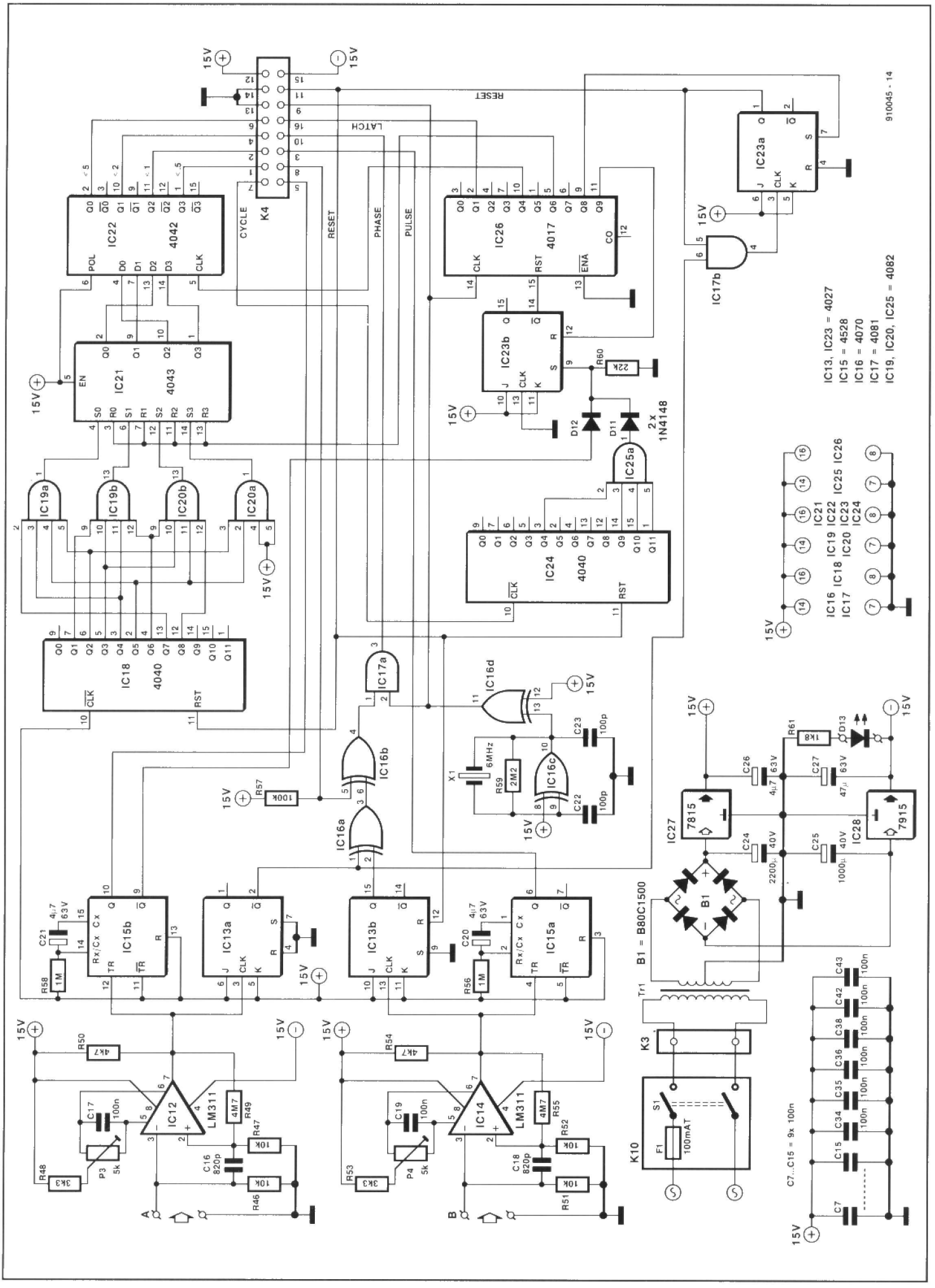


Fig. 4. Diagram of the circuit contained on the mother board.

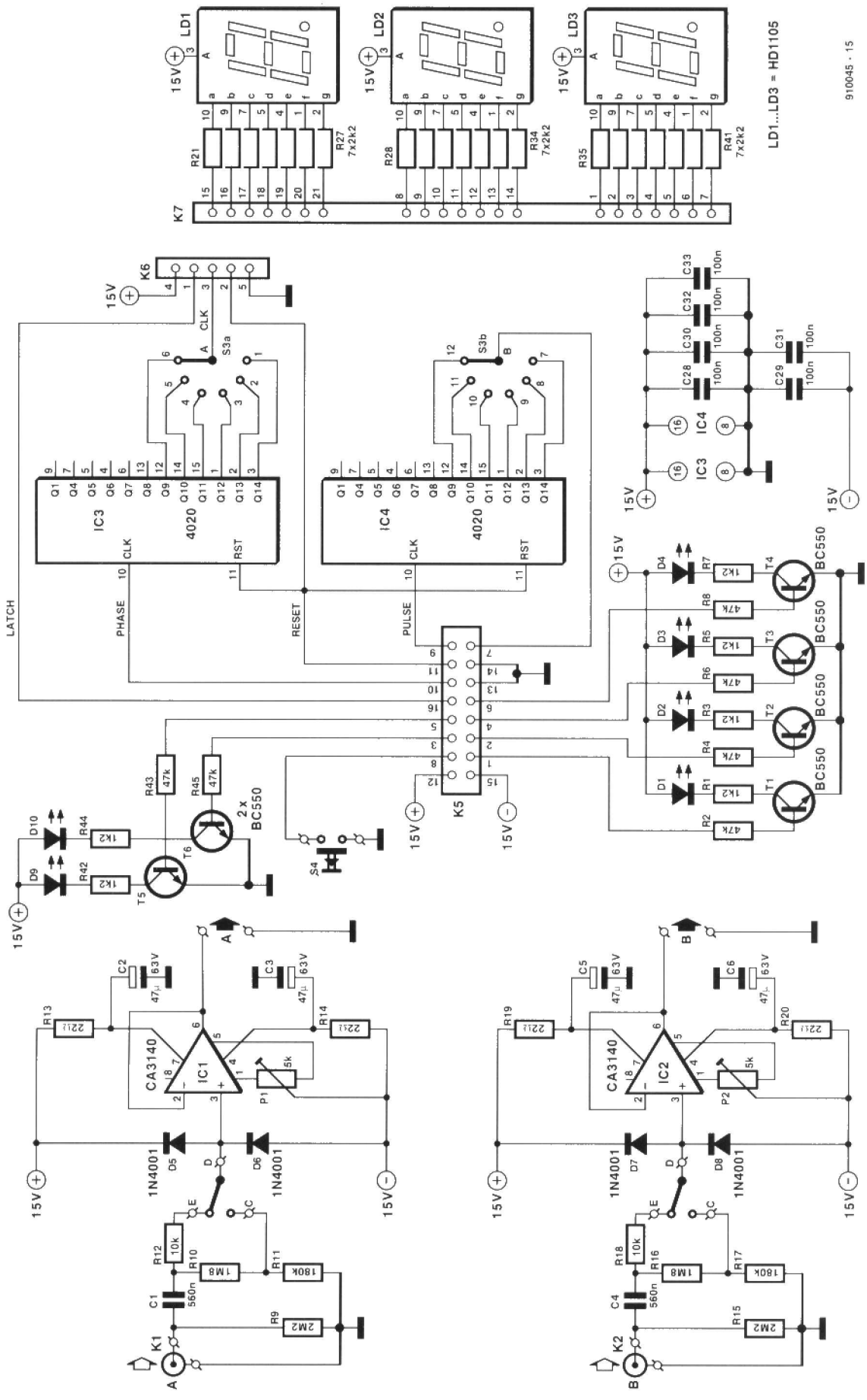


Fig. 5. Diagram of the circuit containing the displays, input stages, and selector switches.

opamps is compensated by presets P_3 and P_4 respectively. Bistables IC_{13a} and IC_{13b} split the digitized signal into a symmetrical signal (duty factor = 50%) that is suitable for measurements.

Monostables IC_{15a} and IC_{15b} actuate the LEDs (D_9 and D_{10}) on the front panel to indicate that suitable signals are input. At the same time, IC_{15b} enables the reference counter via its Q output.

The outputs of IC_{13a} and IC_{13b} are combined via XOR gate IC_{16a}. Another XOR gate, IC_{16b}, and switch S_4 on the front panel make it possible to invert the phase difference as discussed before.

Finally, IC_{17a} combines the output of the phase comparator with the clock frequency (6 MHz). When the output of XOR gate IC_{16a} is high, the clock is passed on and the measurement may be carried out.

The clock signal is generated by a crystal oscillator based on IC_{16c} and buffered by IC_{16d} before it is applied to the relevant stages.

At the end of the measurement, a reset cycle is started by IC_{24}. As soon as this IC has counted 3,600 pulses, IC_{23b} is set via IC_{25a} and OR gate D_{11}–D_{12} and in its turn resets decade scaler IC_{26}. This actuates the latch signal, whereupon the counter state is transferred to the display drivers (further discussed later on). Subsequently, IC_{22} receives a clock pulse and stores data concerning any measurement error, after which IC_{21} is reset. All relevant measurement data are then stored and the remainder of the circuit is reset via bistable IC_{23a}. When the reset cycle is over, IC_{23a} is returned to the relevant output state via AND gate IC_{17b}. At the same time, IC_{24} is reset by the clock pulse that appears at the Q9 output of IC_{26}. The circuit is then ready for the next measurement.

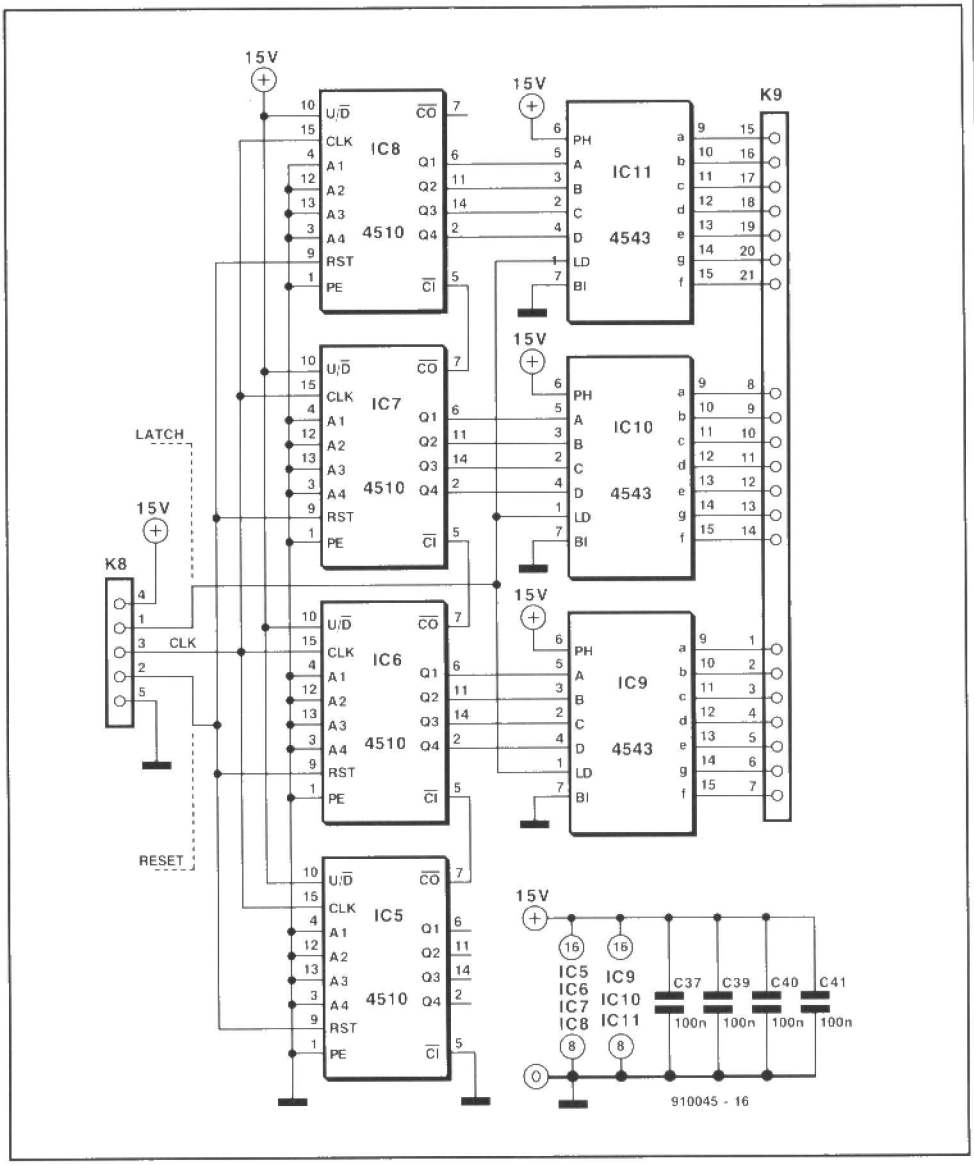


Fig. 6. Diagram of the logic circuits for the LED displays.

PARTS LIST

Resistors:
R1, R3, R5, R7, R42, R44 = 1.2 kΩ
R2, R4, R6, R8, R43, R45 = 47 kΩ
R9, R15, R59 = 2.2 MΩ
R10, R16 = 1.8 MΩ
R11, R17 = 180 kΩ
R12, R18, R46, R47, R51, R52 = 10 kΩ
R13, R14, R19, R20 = 22 Ω
R21–R41 = 2.2 kΩ
R48, R53 = 3.3 kΩ
R49, R55 = 4.7 MΩ
R50, R54 = 4.7 kΩ
R56, R58 = 1 MΩ
R57 = 100 kΩ
R60 = 22 kΩ
R61 = 1.8 kΩ
P1–P4 = 5 kΩ preset

Capacitors:
C1, C4 = 560 nF
C2, C3, C5, C6, C20, C21, C26 = 4.7 µF, 63 V, radial
C7–C15, C17, C19, C28–C44 = 100 nF
C16, C18 = 820 pF
C22, C23 = 100 pF
C24 = 2200 µF, 40 V
C25 = 1000 µF, 40 V
C27 = 47 µF, 40 V, radial

Semiconductors:
D1–D4, D9, D10, D13 = LED, 3 mm
D5–D8 = 1N4001
D11, D12 = 1N4148
B1 = B80C1500
T1–T6 = BC550
IC1, IC2 = CA3140+
IC3, IC4 = 4020
IC5–IC8 = 4510
IC9–IC11 = 4543
IC12, IC14 = LM311DP
IC13, IC23 = 4027
IC15 = 4528
IC16 = 4070
IC17 = 4081
IC18, IC24 = 4040
IC19, IC20, IC25 = 4082
IC21 = 4043
IC22 = 4042
IC26 = 4017
IC27 = 7815
IC28 = 7915

Miscellaneous:
K1, K2 = BNC audio socket
K3 = 2-way terminal block, 7.5 mm centre
K4, K5 = 16-way box header
K10 = mains entry plug with integral fuse holder
S1, S2 = single-pole change-over switch
S3 = rotary switch, 2 poles, 6 positions, for PCB mounting
S4 = SPST switch
X1 = crystal, 6 MHz
LD1–LD3 = HD1105, common anode
Tr1 = mains transformer, 15 V, 18 VA
F1 = fuse, 100 mA, delayed-action
Mains on-off switch
Enclosure (ABS)
Knob for S3
Heat sinks for voltage regulators
PCB 910045-1
PCB 910045-2
PCB 910045-3
Front panel foil 910045-F

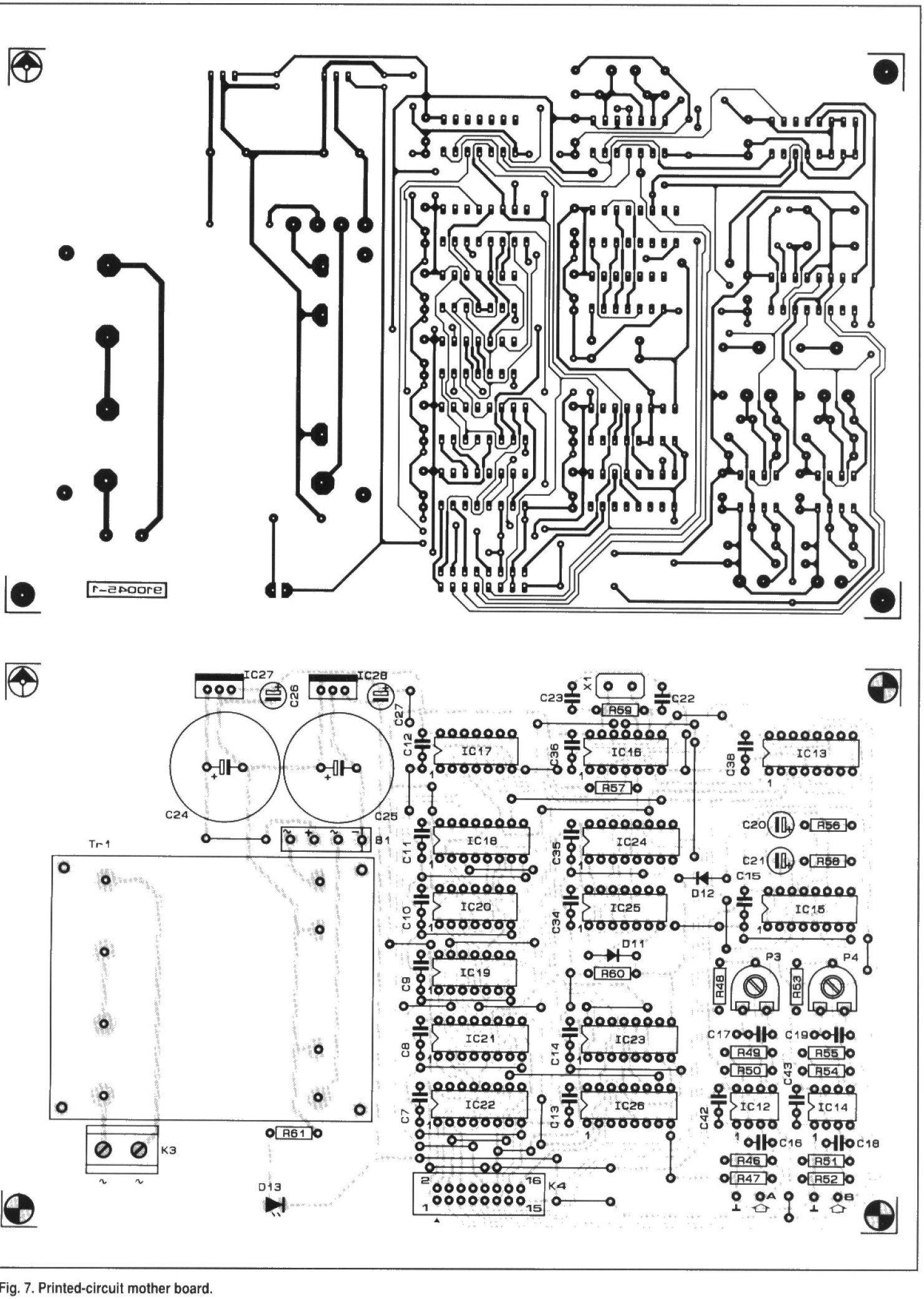


Fig. 7. Printed-circuit mother board.

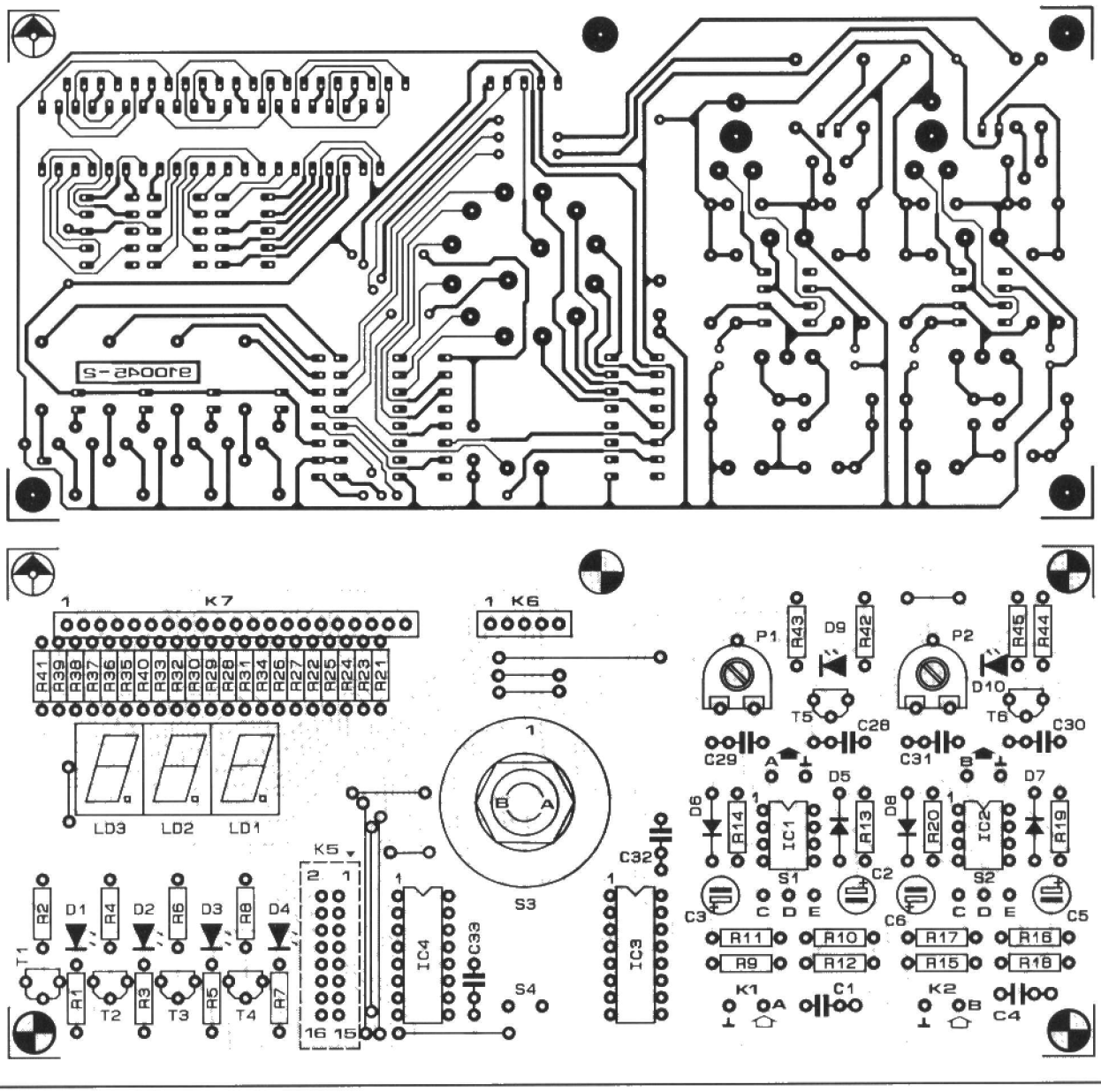


Fig. 8. Printed-circuit board for the displays, input stages, and selector switches.

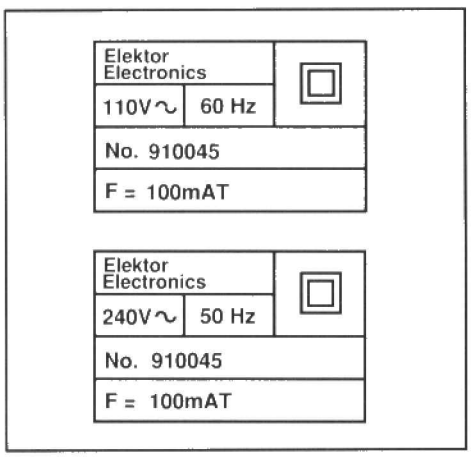


Fig. 9. Suggested labels for the rear panel of the digital phase meter.

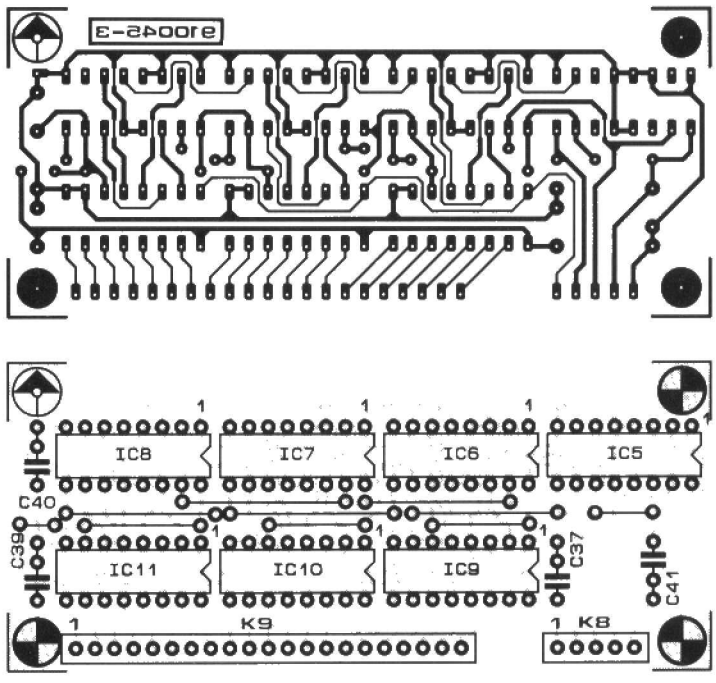


Fig. 10 Printed-circuit board for the logic circuits for the LED displays.

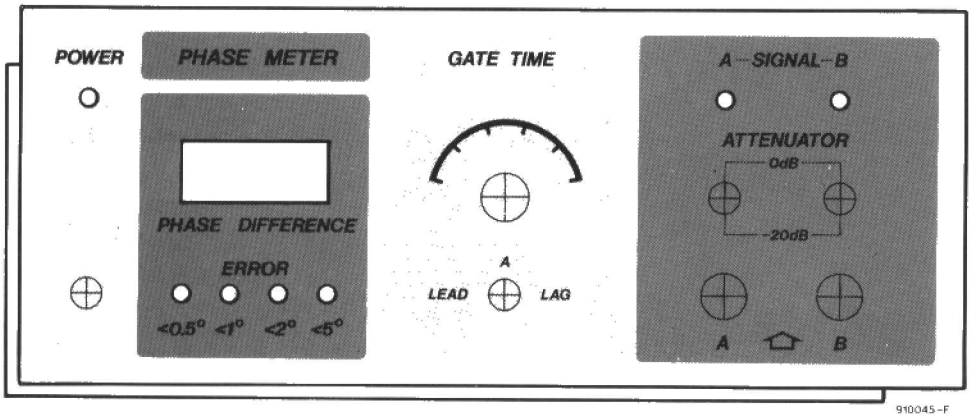


Fig. 11. The front panel foil for the digital phase meter is available through our Readers Services.

As mentioned before, the more periods are used, the more accurate the measurement. The counter in error detector IC_{18} counts the number of periods between the onset of the measurement and the generated latch pulse. Four AND gates decode the result at 360, 180, 90 and 36 periods in one measurement cycle; these counts correspond to errors of 0.5°, 1°, 2°, and 5° respectively. Depending on the number of counted periods, one or more LEDs light; when they all light, the error is negligibly small.

Figure 5 shows the circuit of the displays, the indicators, the input stages and the stage for selecting the measurement duration. The indicator LEDs are driven by transistors: the control lines are connected to relevant points on the mother board via K_5.

The input impedance is about 1 MΩ. Large input signals may be attenuated by 20 dB (S_1 and S_2). All input signals are buffered by Type CA3140 opamps before they are applied to the comparator on the mother board. The inputs of these buffers are protected against overv-voltage by diodes. Presets P_1 and P_2 serve to minimize the offset at the outputs of the opamps.

Circuits IC_3 and IC_4 are programmable 2^n dividers. IC_3 counts the clock pulses passed by AND gate IC_{17a}, that is, the pulses that indicate how long the output of XOR gate IC_{16b} has been high. The number of these pulses depends entirely on the phase shift between the two input signals. IC_4 is the reference counter that receives clock pulses continually.

The scaling factor is set with S_3: it enables the user to select a measurement time that is most suitable for the frequency of the input signal. The error indicators on the display show whether the correct time has been selected.

Figure 6 shows the circuit contained on the third PCB: the seven ICs form the display counter and interface for the LED displays.

The clock pulses to be counted are applied to cascaded counters IC_5–IC_8 via pin 3 of K_8.

As soon as the latch signal is active, the counter state is stored in display drivers IC_9–IC_{11}. The displays, connected with this part of the circuit via K_9, light to show the correct value measured.

The facilities of setting a pre-determined value and choosing up- or down-counting in the Type 4510 ICs are not used.

At the reset command at pin 2 of K_8 the counters are returned to zero and a new measurement cycle can be started. The previous measurement value is retained on the displays because the display drivers are not reset. The next measurement is thus carried out while the displays show the previous result.

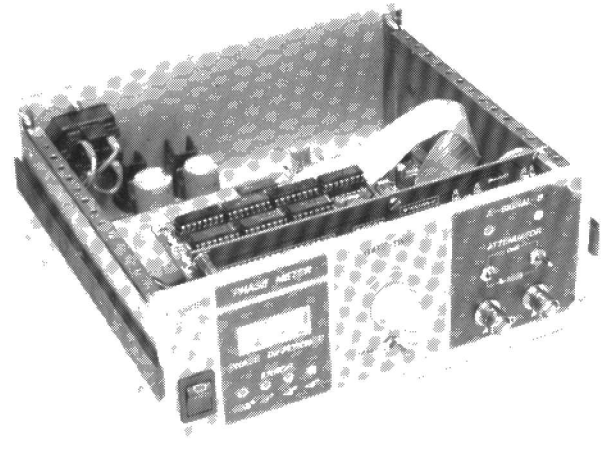


Fig. 12. This photograph of the completed digital phase meter shows how the PCB of Fig. 9 is fitted to the PCB in Fig. 8.

Construction

The three PCBs are shown in Fig. 7, 8, and 10. Their population is straightforward, but it is best to begin with boards 2 and 3. Note that the box header on board 2 must be soldered at the track side. Connectors K_8 and K_9 on board 3 may be replaced by right-angle print headers. As a bonus, such headers would ensure a firm mechanical link between boards 2 and 3. In any case, the boards are provided with holes to enable corner braces to be used for strong mechanical interlinking.

Mount the LED displays on board 2 about 1 cm ($^3/_8$ in) above the board with the aid of wire-wrap IC sockets.

Connect switches S_1, S_2, and S_4, to the board with short lengths of wire; fit S_3 directly to the board.

Cut the terminal wires of D_1–D_4, and D_9 and D_{10} to about 2 cm ($^{13}/_{16}$ in): this will ensure that they will be located exactly behind the windows in the fron t panel.

Fit soldering pins at A and B and adjacent earth points at the track side of board 2.

The power-on indicator, D_{13}, is best fitted to the front panel with the aid of an LED clip or superglue.

Fit board 2 on suitable spacers directly behind the front panel. Just prior to tightening the screws, connect the input sockets to the board via short wires. Next, screw the three toggle switches to the front panel.

Finally, mount board 3 at right angles to the track side of board 2 as shown in the photograph in Fig. 12.

Mount the mother board on the bottom plate of the enclosure, after which all necessary electrical connections to the other boards, the power-on LED, and on-off switch to mains entry plug can be made.

Finally, interlink points A and B, and the associated earthing points, on the mother board and board 2 by single screened audio cable.

TECHNICAL DATA

Measuring range	10 Hz – 20 kHz
Reading	0–360°
Input sensitivity	6 mV peak
Max. input voltage	100 V peak
Attenuation	0 dB or 20 dB
Measurement time	0.3–10 s
Input impedance	1.1 MΩ
Measuring error	≥0.5°

Calibration and use

Calibration of the phase meter is confined to adjusting the four presets.

Short-circuit inputs A and B and adjust P_1 and P_2 for zero output of IC_1 and IC_2.

Remove the short-circuit from the inputs and apply a sinusoidal a.f. signal at a level of about 10 mV to the inputs. Adjust P_3 until comparator IC_{12} toggles exactly at the zero crossing point: check this on an oscilloscope.

Finally, adjust P_4 until the display shows a phase difference of 0°.

Start measuring a phase shift by applying the two signals to the inputs and turning S_3 (gate time) fully clockwise. Then turn the switch anti-clockwise step by step (when the accuracy increases). When the indicator marking a measuring error of 0.5° lights, the optimum position for this measurement has been reached. Since the measurement period increases all the time, it may take a few seconds at low frequencies before the indicator lights. That is, however, the price to be paid for accuracy at low signal frequencies. ■

THE QTC LOOP ANTENNA

The quest for ever reduced sizes of efficient HF transmitting antennas is a compulsive exercise which one has great difficulty in dropping once 'bitten by the bug'. The antenna described here is a new challenge: a directional, compact, table-top loop design with proven excellent performance in the 80-m band.

Richard Q. Marris, G2BZQ

THE lower the HF frequency, the more challenging the idea of being able to use a small antenna. For instance, in the 80 m (3.5 MHz) amateur band, a dipole antenna would be around 42 m long. Many do not have the real estate to accommodate such a dipole, apart from possible planning permission difficulties, and difficulties with leases or neighbours. For apartment dwellers an outside antenna is invariably impossible. For non-amateur applications there are various requirements for discrete and easily portable antennas. As a result, a compact table-top antenna as described here becomes most attractive for many applications.

Small and efficient

Over the years, a number of small table-top HF antennas have been designed, built and air-tested. By far the best has been the spiral loop (Ref. 1) to cover the 3.5 to 3.8 MHz amateur band. This was a very simple 23-inch (approx. 59 cm) diameter octagonal experimental model which I used over the last year with a 7-watt CW transmitter.

It has been useful and fortunate during my experiments that there has been a regular daily 2-way schedule, between 05.00/05.30 a.m. on 3,560 ±5 kHz, with a friend in Stuttgart, Germany. He has entered into the spirit of these experiments, which have proved to be essential, though, of course, much longer distances have been achieved. His transmitter has a power output of about 100 watts feeding an outdoor dipole. As against this, I have been using a spiral loop on a table alongside my low-power transmitter. Strangely enough, looking back over the months, there has been little difference in signal strength reports either way.

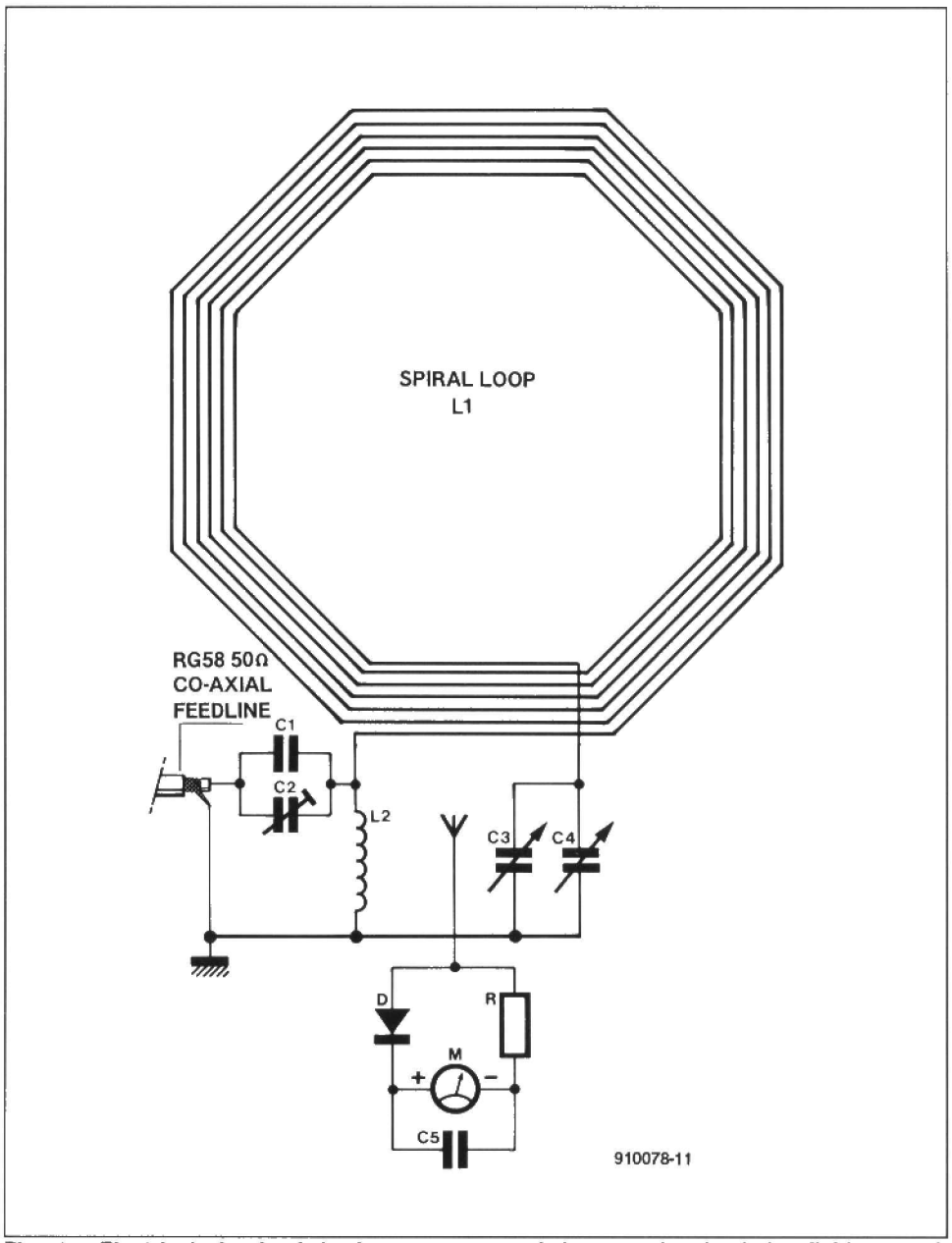


Fig. 1. Electrical circuit of the loop antenna and the associated relative field strength

The tiny amount of textbook information (Ref. 2) available on spiral loops is concerned with direction finding (DF) and not transmission. It is stated that the reception advantages of the spiral loop over a standard box loop, with the turns side-by-side, are mainly greater sensitivity/gain, and a narrower directional polar diagram. Based on experience with the 23-inch diameter spiral loop, and seeking greater efficiency and transmission range, further experiments produced the much more sophisticated and efficient QTC spiral loop. Just in case you do not remember your Q-codes: QTC means "I have a message for you".

The message

is that the new loop antenna has a 30-inch (approx. 76 cm) octagonal configuration, which, although giving as much as 50% increase in loop area, still fits into the table top space available.

The circuit (Fig. 1) shows a 5⅛ turns loop, L_1, plus impedance matching coil, L_2. The inductors are resonated by variable capacitors C_3 and C_4. C_3 sets the band segment to be used, and C_4 is a small bandspread tuner.

A 48-inch (approx. 122 cm) length of RG58 coax cable is fed via C_1 and C_2, in parallel, to the junction of L_1 and L_2. Capacitor C_2 is a preset variable type providing a fine coupling adjustment.

Maximum radiation is on the outer turns of L_1 (H_1–I), and minimum radiation on the inner turns (H_1–E). The radiation pattern (polar diagram) is shown in Fig. 2. It will be realized that the large lobe has to be pointed towards the station to be contacted. In the

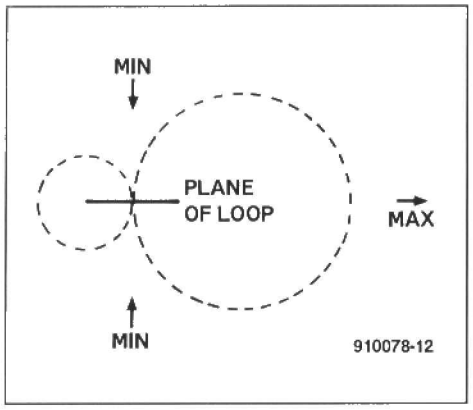


Fig. 2. Theoretical polar radiation pattern of the QTC loop.

author's shack the loop usually stands on a small turntable for simple manual rotation.

The antenna has a built-in tuning meter seen at the bottom of the circuit. This is basically a RF probe of which the sensitivity is reduced to an absolute minimum, so that a 'sample' of the transmitted signal can be taken from the outer turn of L1. The sensitivity of the probe is controlled by the value of resistor *R*, as well as by the length and position of the mini-antenna.

All components are neatly located in a plastic control box as shown in Figs. 3 and 4. The RF meter assembly is mounted in a Terry clip on top of the box, with the diode, the resistor and capacitor C5 wired behind the meter. This method was adopted to enable the tuning assembly to be used on other experimental antenna models.

The complete loop assembly is shown in Fig. 4. When designing such a loop, it is essential that metal parts be avoided, which means that you have to use wood and plastic construction throughout.

Construction

As shown in Figs. 1 and 4, the loop frame consists of eight 'spokes'. These are made of four lengths of moulded hardwood, each 30 inch long, 5/8-inch wide and 1/4-inch thick (approx. 76.2 × 1.6 × 0.6 cm). A 2BA (5 mm) clearance hole is drilled in the centre of each spoke, and after an application of glue, the spokes are clamped together with a 2BA bolt, overlapping in the order illustrated. The whole is given a polyurethane varnish. A 6-way 2-amp polythene terminal block is screwed to the end of each spoke. These provide the necessary spacing and insulation of the wire turns.

A 23 × 0.8 × 0.8-inch (approx. 58.4 × 2 × 2-cm) vertical wooden support is glued and bracketed to a suitable wooden base, the whole being teak wood stained. The loop frame is then glued and bolted to the top of the vertical support.

The loop winding, L1, uses PVC-covered stranded 7/0.2 mm wire with an outside diameter of 1.2 mm and an electrical rating of 1 kV/1.5 A. After loosening all grub screws in the terminal blocks, the wire is threaded through, turn by turn, for 5 1/8 turns starting at the outer left-hand lower frame spoke, and threading through all blocks in a

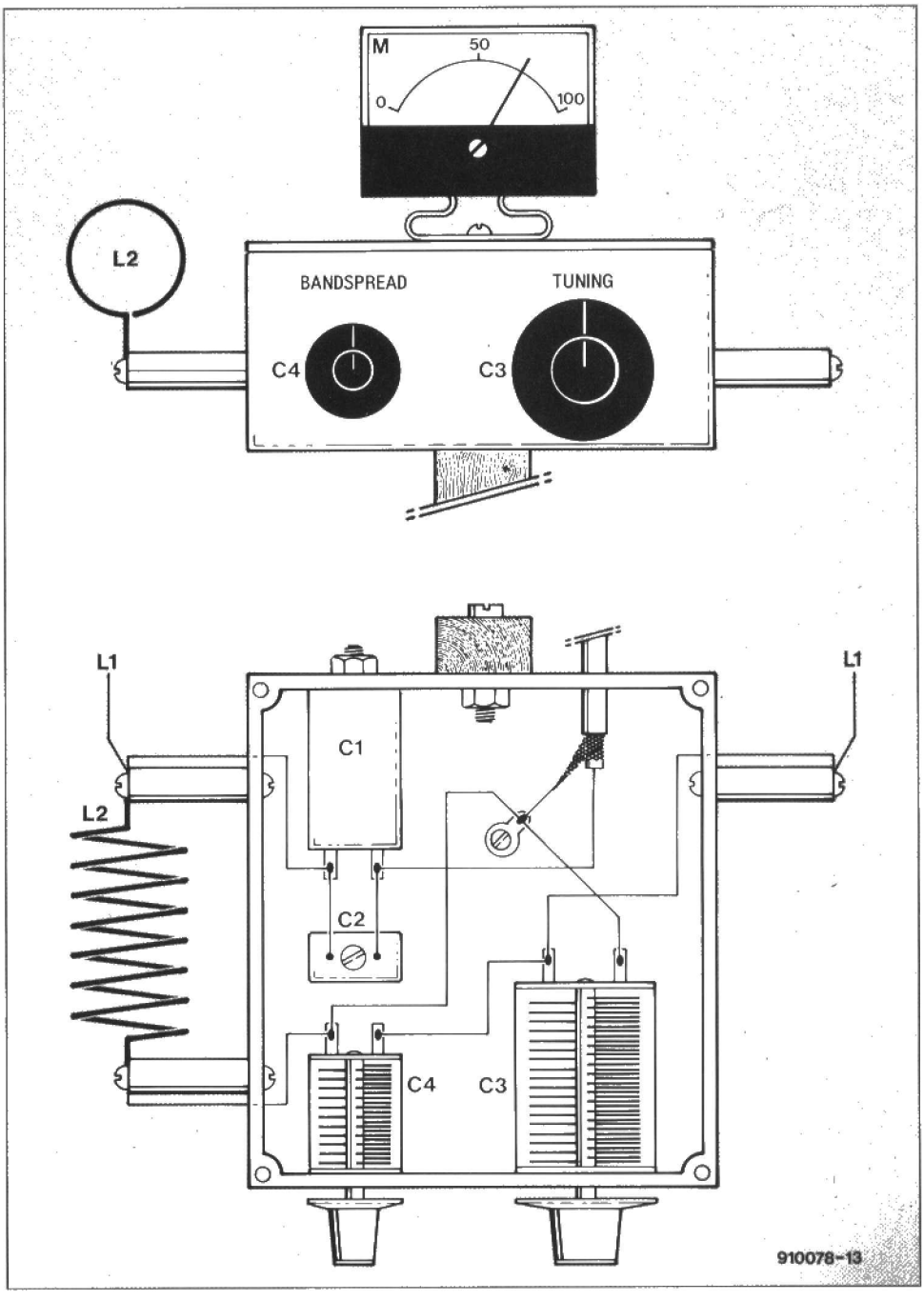
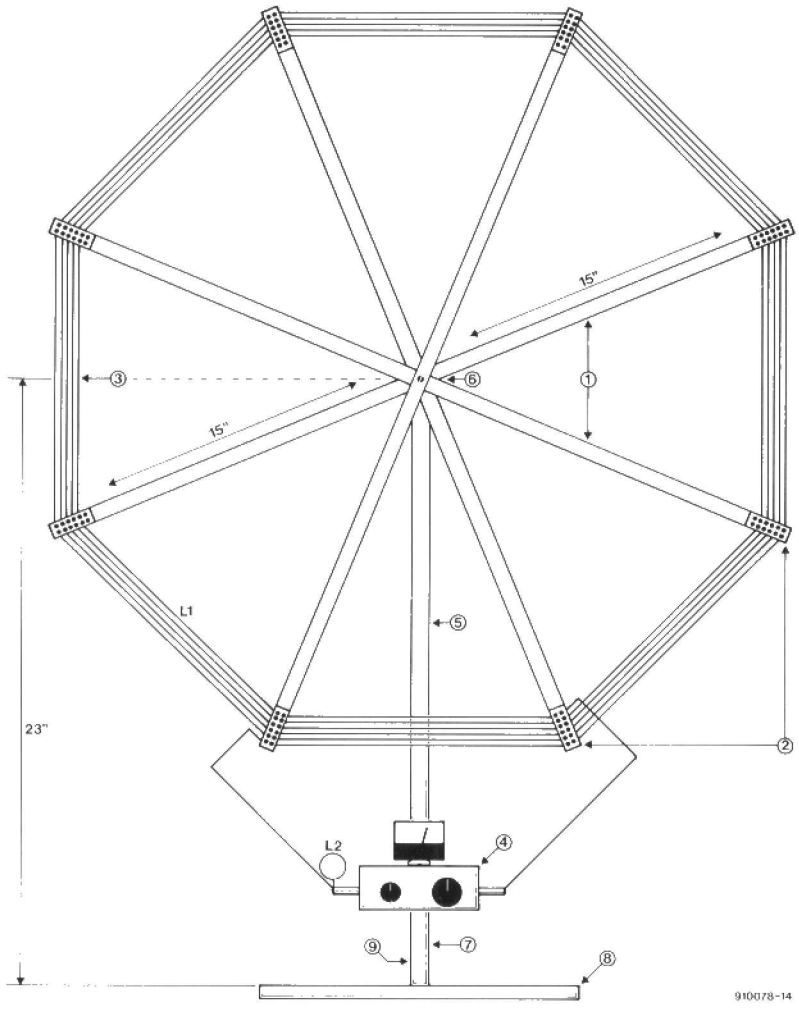


Fig. 3. Mechanical outline of the antenna tuning unit and the field strength indicator.

COMPONENTS LIST

C1 = 3750 pF 500V silver-mica capacitor.
C2 = 100 pF preset capacitor (Jackson C803).
C3 = 75 pF variable capacitor (Jackson C809), plus knob.
C4 = 12.7 pF variable capacitor (Jackson C16), plus knob.
C5 = 22 nF mica capacitor.
M = 250 µA f.s.d. 40 × 40 mm moving coil meter (Maplin LB808).
D = HF silicon diode.
R = 1 kΩ resistor (see text).
L1 = 5 1/8 turns of PVC covered stranded 7/0.2 mm wire. Outside diameter: 1.2 mm, 1 kV/1.5 A rating (see text).
L2 = 13 turns 16SWG tinned wire, 1 inch internal diameter (see text).
Feedline = 48 inch RG58 coaxial cable, plus plug to suit transmitter.
Box = ABS box type MB3, 118 × 96 × 45 mm. Maplin ref. LH22.
Terminal blocks = qty. 4 12-way 2 amp terminal block. Maplin ref. FE78.
Spacers = qty. 3 insulated spacer type M3, 30 mm long, Maplin ref. FS40T.
Spokes = qty. 4 8-foot lengths of 5/8 × 1/4 inch moulded hardwood (DIY store).
Vertical support = 23 × 0.8 × 0.8 inch wood (DIY store).
Wood base = 12 × 8 × 0.5 inch plywood or similar.
2 1/2 inch steel support bracket.



1. 4 lengths moulded hardwood 30" × 5/8" × 1/4". Varnished. 2BA holes drilled in the centre. Glued and bolted together.
2. 8 off 6-way 2-amp polythene terminal blocks used as insulated wire spacers.
3. 5⅛ turns of PVC stranded wire (for specs see components list).
4. See Fig. 3.
5. Wood vertical support 23" × 0.8" × 0.8", wood stained.
6. 2" × 2BA bolt.
7. Box front vertical support, 4½" × ½" × ¾", wood stained.
8. Wood base 12" × 8" × ½" (or similar), wood stained.
9. 2½ steel support bracket behind wood vertical support.
10. Drilled and secured with glue and c/s wood screws.

Note: " = inch = 2.54 cm.

Fig. 4. The construction of the antenna is based on commonly available parts and materials. The 'spokes' are bolted and glued together in the centre.

reducing anti-clockwise spiral. The loop is terminated at the inner of the lower right-hand spoke, as shown in Fig. 4. Wire tails are left at the loop ends for cutting and connecting later. After tightening the loop turns, the insert screws in the terminal blocks are tightened sufficiently to keep the turns straight.

After fitting the variable capacitors and insulating pillars in the box (Fig. 3), the box is bolted to the main vertical support. An extra, smaller, vertical wood member secures the box front to the wood base with screws and glue. The meter assembly is secured to the font lid of the box lid with the aid of a large plastic-coated Terry clip. The RG58 coaxial feedline enters the box at the rear (Fig. 3), and is cleated down to the vertical support and along the wood.

Inductor L2 is soldered to tags on the two left-hand insulated pillars. It consists of 13 turns of 16SWG (16AWG, approx. 0.6 mm dia.) tinned copper wire wound to 1 inch (2.54 cm) diameter. The turns are then spaced to about 1.5 times the wire thickness. The whole loop assembly is now wired as shown in Figs. 1, 3 and 4.

Testing and operation

Initial tests are made with a receiver. On the prototype with the bandspread, C4, at mid capacity, it was found that by rotating C3 the frequency range was 2,500 kHz to 4,500 kHz, which adequately covers the 80-m band (3,500 to 3,800 kHz), with some overlap. In the USA and elsewhere, the 80-m band is extended to 4,000 kHz. Resonance is indicated by a peak of noise and signal strength in the receiver. The radiation pattern can be checked on a selected signal by rotating the loop for maximum signal strength. From Fig. 2 it will be seen that this coincides with the large lobe. Further rotation of the loop through 360 degrees gives a radiation pattern as shown.

In practice, C4 is set to minimum capacitance, and C3 is tuned to start of the selected band segment. For instance, if the required operating segment is 3,500 to 3,800 kHz, C3 is set to about 3,600 kHz (with C4 at minimum capacitance). Bandspread control C4 is then used to tune the loop, giving fine tuning over 3,500 to 3,600 kHz, and so on.

The transmitter adjustment is as follows:

1. Connect the transmitter to a 50-Ω dummy load. Set the transmitter to the selected frequency and adjust the P.A. for optimum loading.
2. Remove the dummy load and substitute the loop.
3. Resonate C4 to the transmitter frequency, and peak the coupling preset adjustment, C1.
4. It should be possible to use the transmitter at ±20 kHz of the setting up frequency without retuning the loop with C4. Minor adjustments of C4 will easily retune the loop outside this bandwidth, as required.

Proceed with the adjustment of the tuning meter. The mini-antenna consists of a few turns of stiff wire wound around a pencil. Remove the wire from the pencil, and position the end of it directly under the bottom turn of L1. The mini antenna is manipulated up and down so that the meter reads about ¾ full-scale when the transmitter is correctly loaded. When retuning the transmitter during operation, the meter should always peak around this point, provided the transmitter power is unaltered. Note, however, that the sensitivity of the meter depends also on the value of resistor *R* and the transmitter power. The value shown, 1 kΩ, is satisfactory for a transmitter power of about 5 to 10 watts. For higher or lower power transmitters, the value of *R* is changed experimentally.

When operating the antenna it should be kept a loop diameter away from walls, pipes and electrical wiring. It will be noticed that due to the loop directivity the received level of interference is well down on a normal antenna. Best results will be obtained when the large radiation lobe is pointed directly at the station being contacted.

Finally, note that the loop antenna is intended as a low-power device for indoor use. In the interest of safety, a transmitter power of 20 watts should not be exceeded. No doubt the design could be re-engineered for higher power and outdoor use. ■

References:

1. "The Miser's T/R loop antenna" by R.Q. Marris, *Elektor Electronics* November 1990.
2. The Admiralty handbook of Wireless Telegraphy, Volume 2, 1938.

For further reading:

- The ARRL Antenna Book, 14th edition.
- Antennas (2nd edition), 1988, by John D. Kraus (McGraw-Hill).

INTERMEDIATE PROJECT

A series of projects for the not-so-experienced constructor. Although each article will describe in detail the operation, use, construction and, where relevant, the underlying theory of the project, constructors will, none the less, require an elementary knowledge of electronic engineering. Each project in the series will be based on inexpensive and commonly available parts.

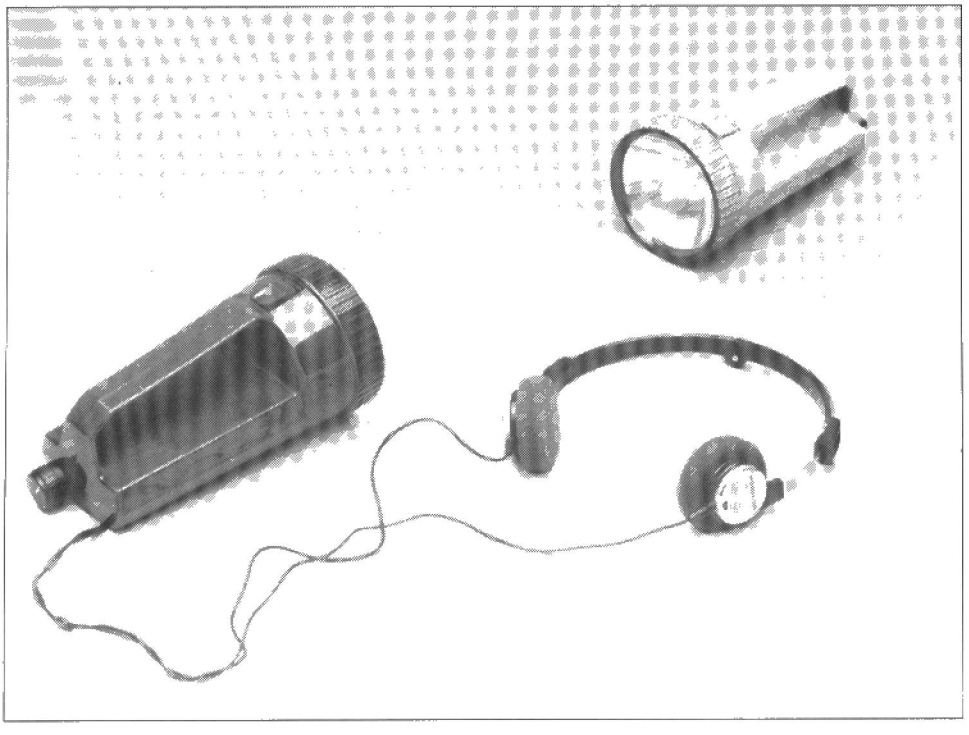
LIGHT TRANSMITTER/RECEIVER

This month we present an experimental circuit to demonstrate that visible light can be modulated and used as a carrier to convey information. Depending on the power of the bulb you use, and the optics for the transmitter and the receiver, this low-cost communication system will carry speech signals over distances of tens to hundreds of metres.

T. Giffard

IN principle, the intensity of a light beam from an electrical source, such as a bulb, can be used as a carrier to convey an audio signal from one point to another. This type of amplitude modulation (AM) can be achieved by using the audio signal to vary the voltage applied to the bulb. The light transceiver described here is intended as an introduction to wireless communication using amplitude modulation. The circuits have been kept simple and can be assembled and put to use in single evening or a rainy afternoon. When used for an experiment rather than a fixed communication link, the transceiver can be even simpler than shown here because existing amplifiers may be used.

Compared to, say, an infra-red emitter there are certain restrictions to the use of common low-voltage bulbs as light sources for an AM-based communication link, and the modulation will not be perfect. Still, the quality of the system will be good enough for a reliable voice link.



On modulation and filaments

Modulating the light intensity of a bulb is not so difficult. However, the relation between the intensity and the filament voltage is not quite as linear as we would like. In practice, the best results are obtained with low-voltage bulbs that have a thin, straight filament. These bulbs, which are used in bicycle rear lights, have a relatively rapid response to filament voltage variations, and are therefore capable of 'following' a speech or music signal.

The response of a bulb to sine-wave modulation can be significantly improved by applying a direct voltage to the filament, and superimposing the sine-wave. In practice, the best results are obtained with the fixed voltage set such that the bulb lights at half the nominal intensity. This also sets the maximum value of the applied alternating voltage, whose peak value may not exceed the direct voltage. When the voltages are equal, the modulation depth is 100%. In the absence of an alternating voltage component, the modulation depth is 0%.

The light transmitter

The circuit of the light transmitter is shown at the left in Fig. 1. It supplies the light source, bulb La1, with a direct voltage as well

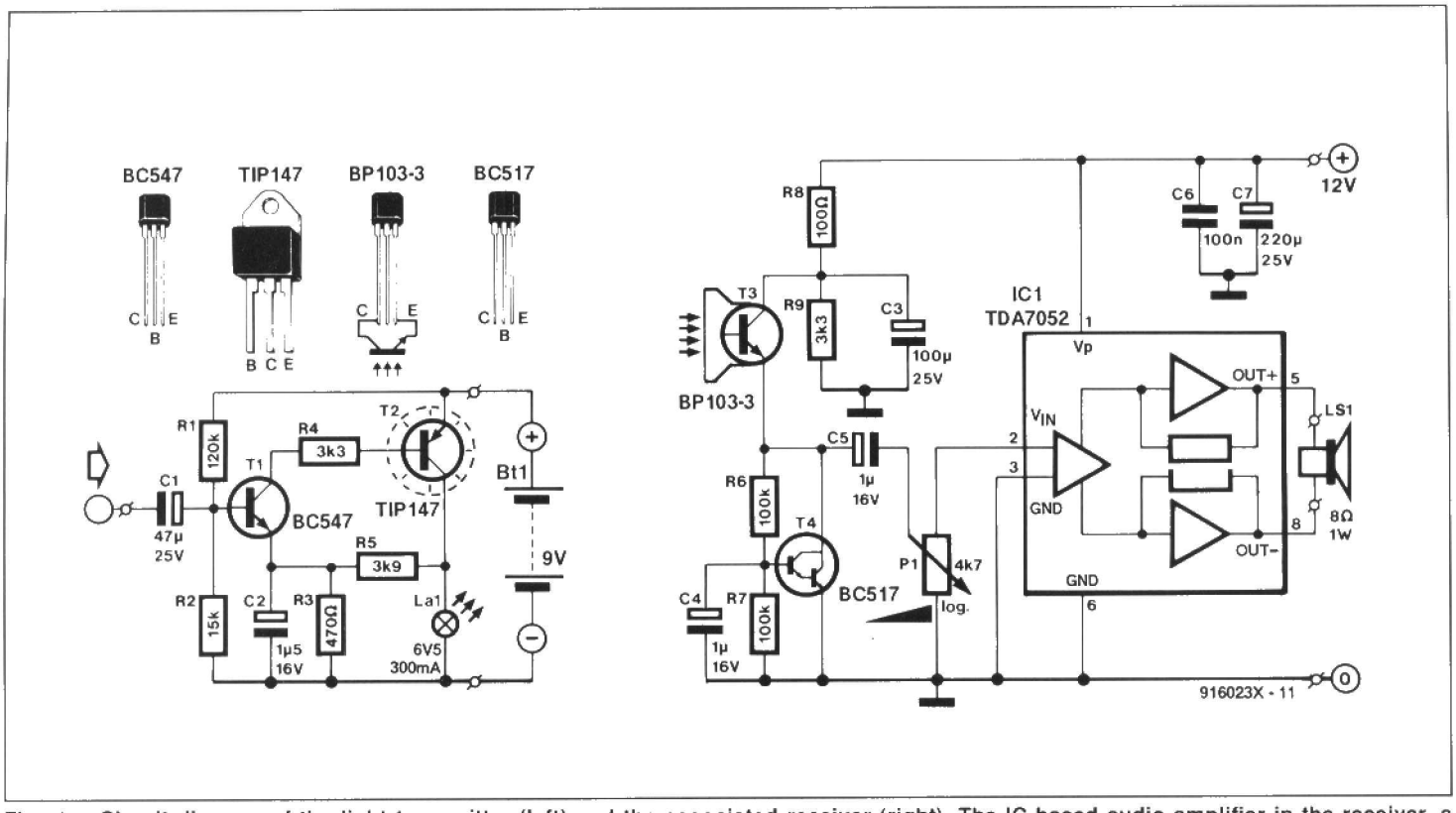


Fig. 1. Circuit diagram of the light transmitter (left) and the associated receiver (right). The IC-based audio amplifier in the receiver, a TDA7052, is optional and may be replaced by any other amplifier you may have available.

as with the modulation signal. The bulb is connected in the collector line of a medium-power transistor, T_2, which functions as an amplifier. When there is no input signal, the collector of T_2 is at about half the supply voltage. An audio input signal applied to the base of T_2 causes the collector voltage to swing between 0 V and the supply voltage. This ensures that La_1 is supplied with the optimum voltage for amplitude modulation.

Transistor T_1 raises the audio input signal and at the same time keeps the quiescent voltage across La_1 at about half the supply voltage. The transistor monitors the collector voltage of T_2 via resistor R_5, and controls the base voltage of T_2 accordingly. A decoupling capacitor, C_2, prevents T_1 acting on the modulation voltage at the collector of T_2. The voltage control is effective only when the average collector voltage of T_2 is no longer correct. The operation of this type of feed-

COMPONENTS LIST

Resistors:

1	120kΩ	R1
1	15kΩ	R2
1	470Ω	R3
2	3kΩ3	R4;R9
1	3kΩ9	R5
2	100kΩ	R6;R7
1	100Ω	R8
1	4kΩ7 log. potentiometer	P1

Capacitors:

1	47µF 25V radial	C1
1	1µF5 16V radial	C2
1	100µF 25V radial	C3
2	1µF 16V radial	C4;C5
1	100nF	C6
1	220µF 25V radial	C7

Semiconductors:

1	BC547	T1
1	TIP147	T2
1	BP103-3	T3
1	BC517	T4
1	TDA7052	IC1

Miscellaneous:

1	8Ω 1W loudspeaker	LS1
1	6.5V 0.3A bulb	La1
1	Heat-sink for T2	
2	Printed-circuit board	UPBS-1

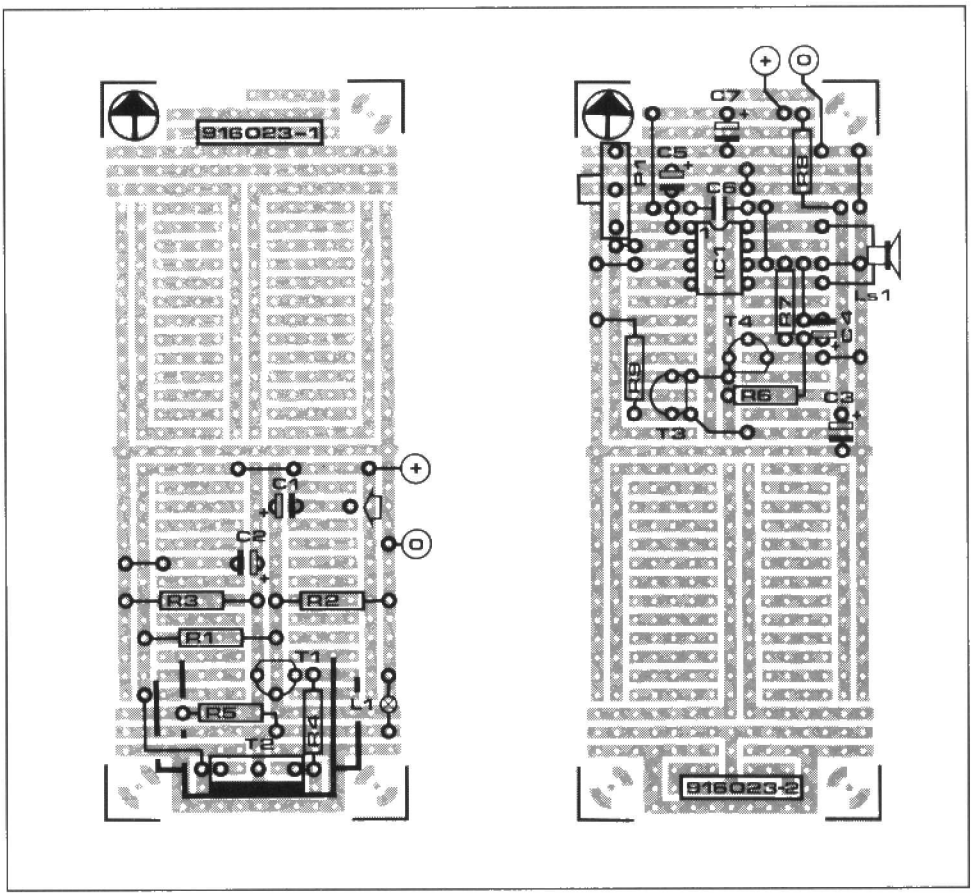


Fig. 2. Component mounting plans of the transmitter (left) and the receiver (right). Both are built on ready-made prototyping boards (see the components list).

back is fairly simple. Assuming that the collector voltage of T2 drops, R5 supplies a lower voltage at the emitter of T1. Since the base voltage of T1 is fixed with the aid of a voltage divider, R1-R2, the transistor starts to draw more collector current, resulting in more current fed into the base of T2. Consequently, the collector current of T2 rises, so that the collector voltage rises also. In this way the initial voltage drop is counteracted and the bulb voltage held constant at about 4.5 V.

The light receiver

The main component in the circuit of the light receiver (shown at the right in Fig. 1) is a photo transistor, T3. The collector current of this transistor is a function of the intensity of the light incident on the device. If the incident light is produced by the light transmitter, the emitter voltage of T3 is a copy of the modulation signal applied to the transmitter. The demodulated signal is fed to a small a.f. amplifier, IC1, via coupling capacitor C5 and volume control P1. The a.f. amplifier, a TDA7052, has a voltage gain of about 100.

Returning to the phototransistor, the emitter potential is held constant by a voltage source based on T4. Assuming that the emitter voltage of T3 rises, the base current of T4 rises via resistor R6. Consequently, the collector current of T4 rises, so that the collector voltage drops. This keeps the emitter voltage of the photodiode in check. Like C2 in the transmitter, C4 prevents the voltage stabilizer acting on the modulation signal, which changes much faster than the average emitter voltage of the photodiode.

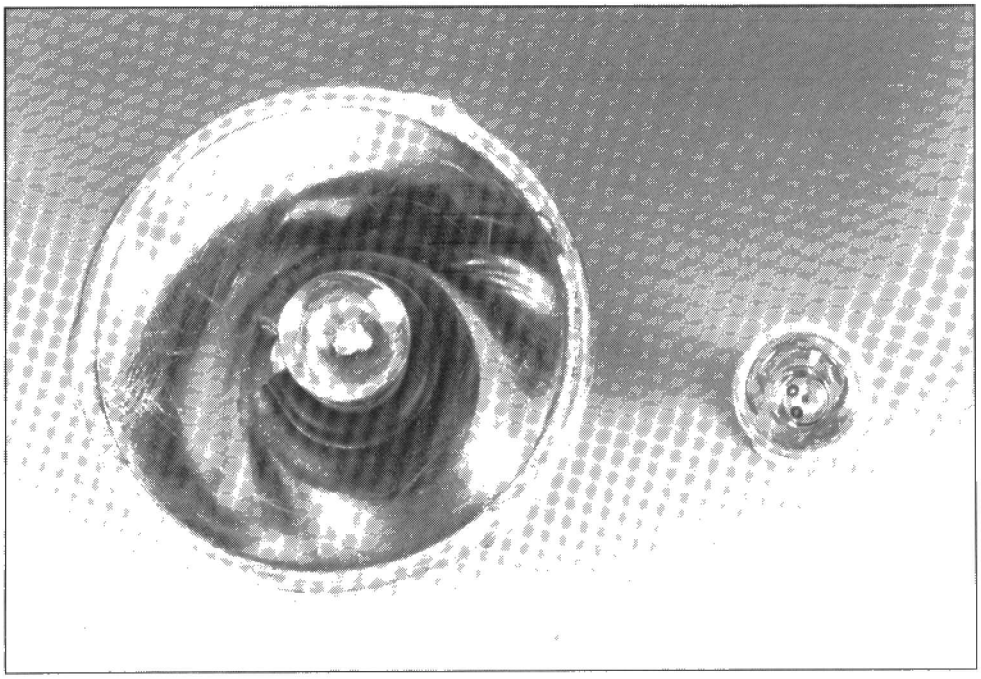


Fig. 4. The transmitter uses a plastic reflector from a pocket torch, while the phototransistor in the receiver is fitted in a reflector of a type normally used for infra-red emitters.

Construction and use

The transmitter and receiver circuits are so simple that they are easily constructed on prototyping boards as shown in Fig. 2. If you want to make a duplex system where each 'station' consists of a transmitter and a receiver, you will require two prototyping boards (order code UPBS-1). For a one-way light link, a single board may be cut in two to accommodate the transmitter and receiver circuit. The photographs in Fig. 3 show the transmitter and the receiver built on two prototyping boards.

There are several options for the construction of the optics. At the transmitter side, you may use a reflector from a torch (see Fig. 4). At the receiver side, a concave reflector is used of the type found on infra-red remote controls. In most cases, the BP103 phototransistor will fit in the opening for an infra-red LED. It will be clear that the distance covered by the system will depend on the size of the optics used. In general, the larger the diameter of the reflectors, the better (an example of the use of car headlight and a magnifying glass for a long-range infra-red communication system is given in Ref. 1). A few prototypes with different coverage were built in torches as shown in the introductory photograph.

You may also want to experiment with the wattage of the bulb used in the transmitter. Note, however, that relatively high bulb powers require T2 to be fitted with a heatsink.

The transmitter draws a relatively high current, and is best powered by a regulated supply or a rechargeable 9-V battery block. The receiver has a very modest power consumption, and can be supplied from a small mains adapter. In some cases, however, such an adapter may produce an unacceptable hum level in the receiver. Fortunately, the hum is simple to suppress by fitting larger supply decoupling capacitors in positions C3 and C7.

Finally, note that the bulb in the transmitter will emit visible as well as infra-red light. This allows you to use an infra-red sensitive phototransistor such as the BPW40 if the BP103 proves difficult to obtain. ■

Reference:

1. "Long-range infra-red transceiver". *Elektor Electronics* November 1987.

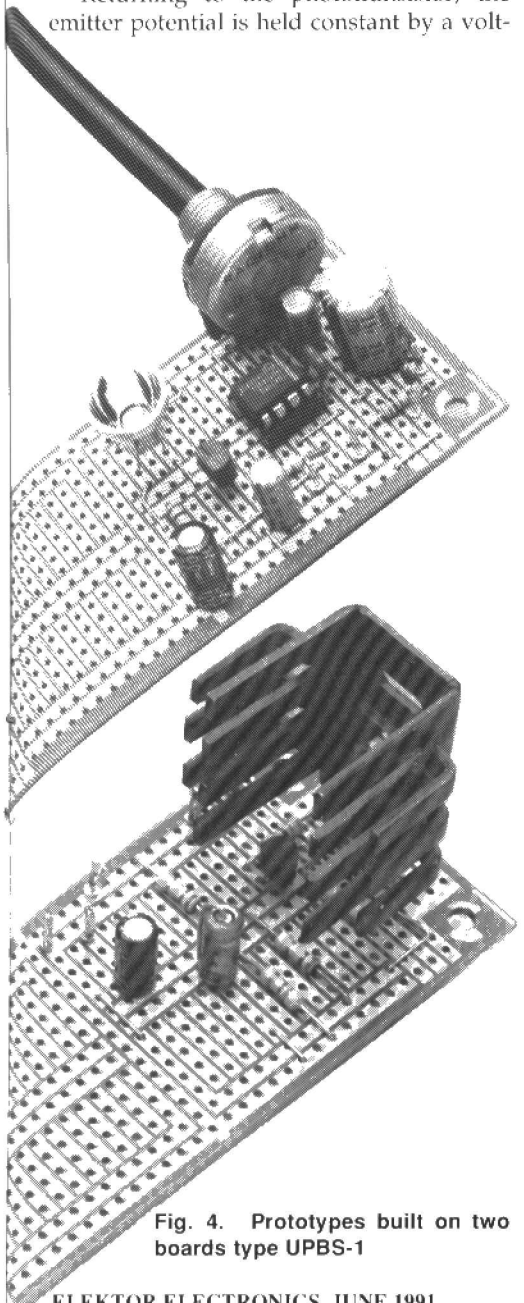
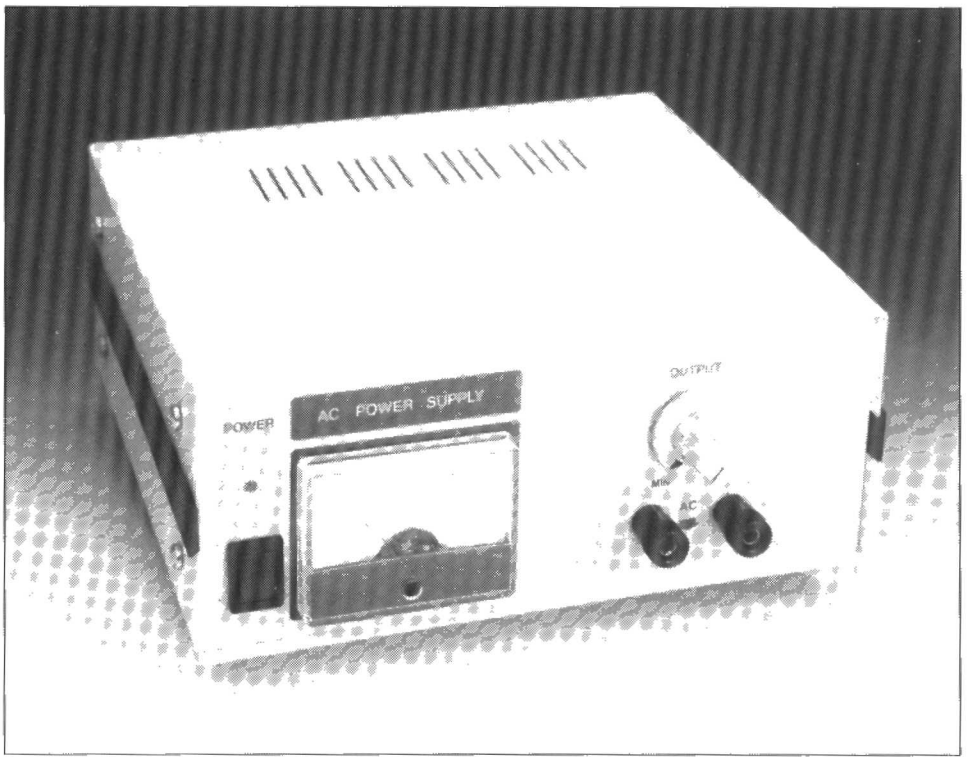


Fig. 4. Prototypes built on two boards type UPBS-1

VARIABLE A.C. POWER SUPPLY

Stabilized and regulated d.c. power supplies are readily available in many shapes and sizes. By contrast, a regulated and perhaps even stabilized a.c. power supply is difficult to find at a reasonable price. The adjustable transformer is in many cases the only alternative, but it, too, is pretty expensive. In this article we present a simple 25-V 1-A a.c. power supply that deserves a fixed place on any electronics workbench.



L. Lemon

AN alternating voltage is much more difficult to stabilize than a direct voltage. In fact, there are two quantities that must be stabilized: the voltage proper (or its amplitude), and the frequency. Since it was intended to keep the present supply as simple as possible, frequency stabilization is not provided. The mains frequency is used here because it is fairly stable and suitable for most applications.

Block diagram

The operating principle of the present supply is to stabilize an alternating voltage with the aid of an adjustable potential divider. As shown in the block diagram in Fig. 1, the potential divider is controlled electronically, and forms part of a regulation loop. A power transistor is used as an adjustable resistor in a diode bridge. The bridge is required because the transistor can handle direct current only. Unfortunately, it has two disadvantages: first, it introduces a voltage loss of two times the forward diode voltage; second, because of their threshold voltage, the diodes do not conduct around the zero crossing of the alternating voltage. As shown in the oscilloscope photograph in Fig. 2, the thresholds cause small flattened parts around the zero crossing of the output voltage. In amplifier terminology this effect is known as cross-over distortion. Fortunately, the effect is of little consequence here, and it can be tolerated bearing in mind that we set out to de-

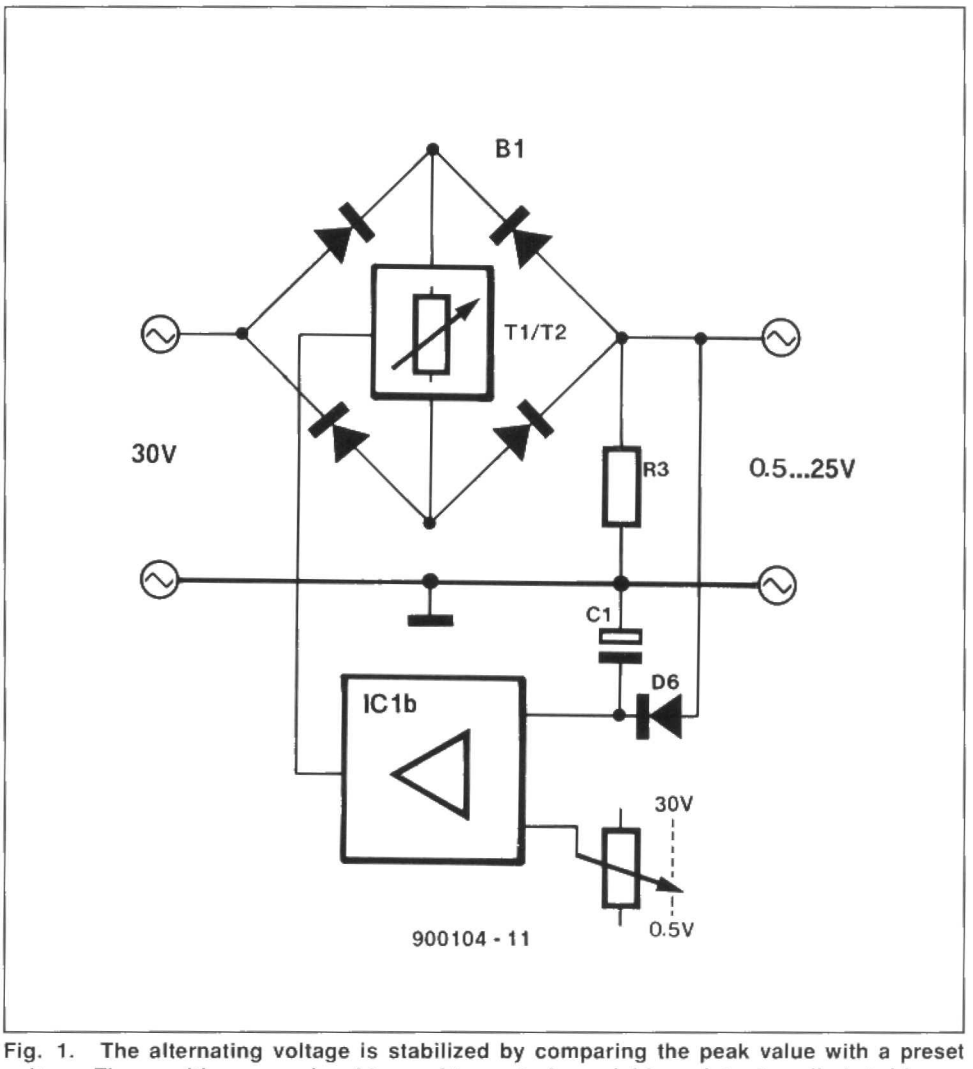


Fig. 1. The alternating voltage is stabilized by comparing the peak value with a preset voltage. The resulting error signal is used to control a variable resistor in a diode bridge.

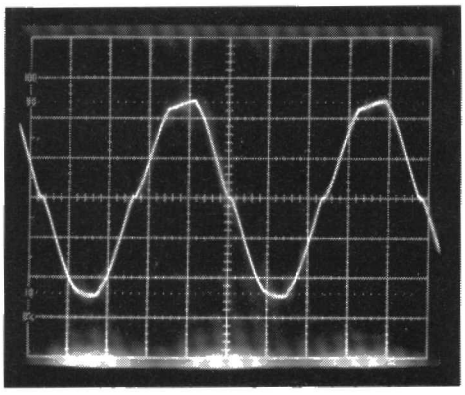


Fig. 2. Output waveform of the power supply. The cross-over distortion is caused by the small forward drop across the diodes in the rectifier bridge.

sign a simple a.c. power supply. Along this train of thought, the supply is based on measuring the peak value of the output voltage, rather than the instantaneous voltage, which is far more difficult. The peak voltage exists across C1, which is charged by rectifier D6. A difference amplifier compares the measured peak value with the value set by the output voltage control, potentiometer P2. Differences between the two voltages cause an error signal that serves to adjust the output voltage until the difference is zero, i.e., until the set output voltage is achieved.

Circuit description

The circuit diagram of the variable a.c. power supply is fairly simple — see Fig. 3. The alternating voltage circuit is almost identical with the block diagram. The diode bridge is formed by a bridge rectifier Type B80C3200/2200 (80 V p.i.v., 3.2 A peak, 2.2 A continuous), and the adjustable resistor by transistors T1-T2. Resistor R3 completes the potential divider.

The voltage control circuit is a little more complex than suggested by the block diagram. The peak voltage rectifier, D6-C1, is followed by a potential divider, R4-R5. This prevents the voltage across C1 exceeding the supply voltage of IC1a (the peak value of a 25-V alternating voltage is much greater than 12 V). The output voltage is indicated by a moving-coil meter, M1, which is calibrated for 25-V f.s.d. (full-scale deflection) by preset P1.

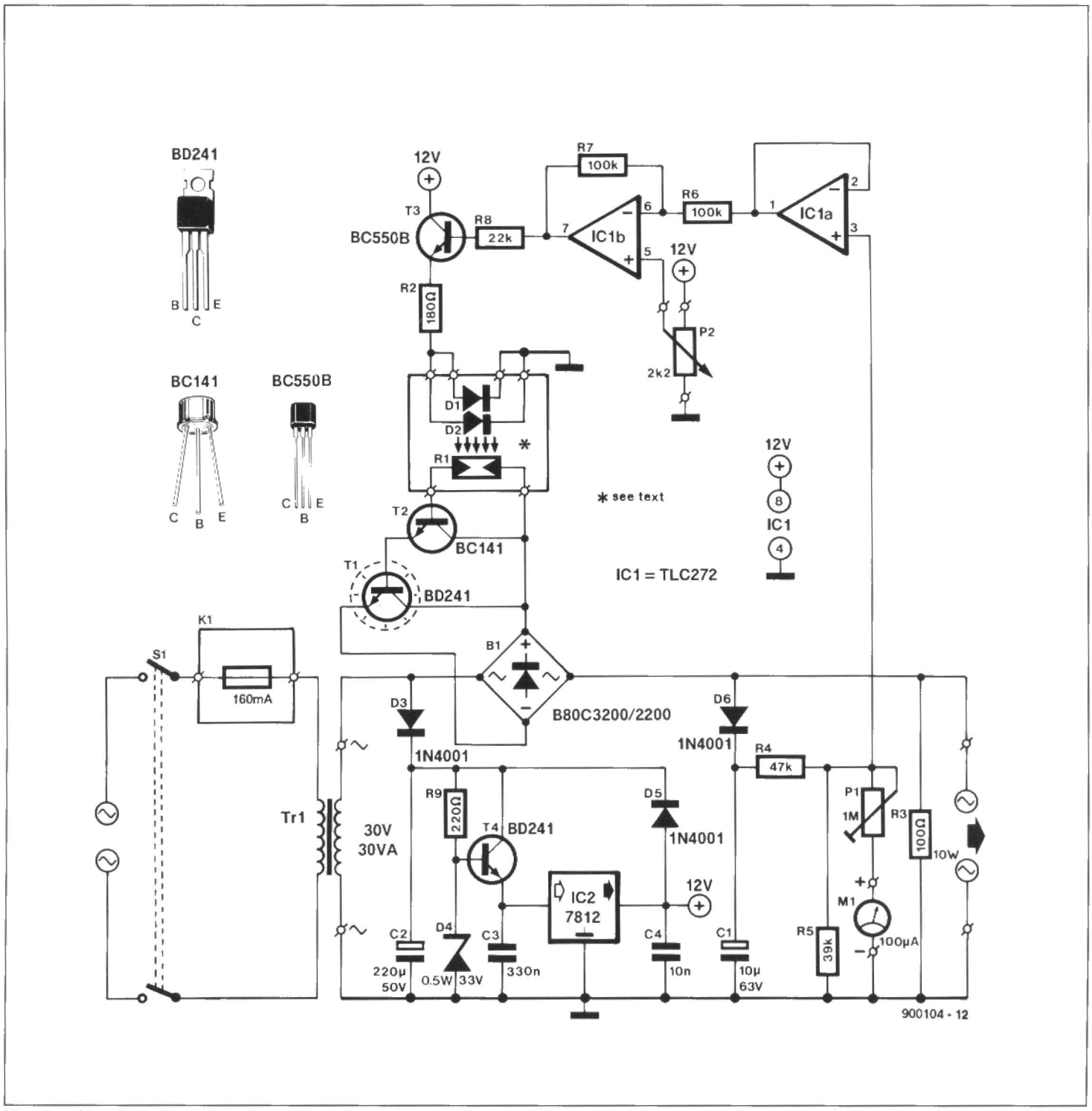


Fig. 3. Circuit diagram of the a.c. power supply. The optocoupler shown here is a home-made type consisting of two LEDs and an LDR.

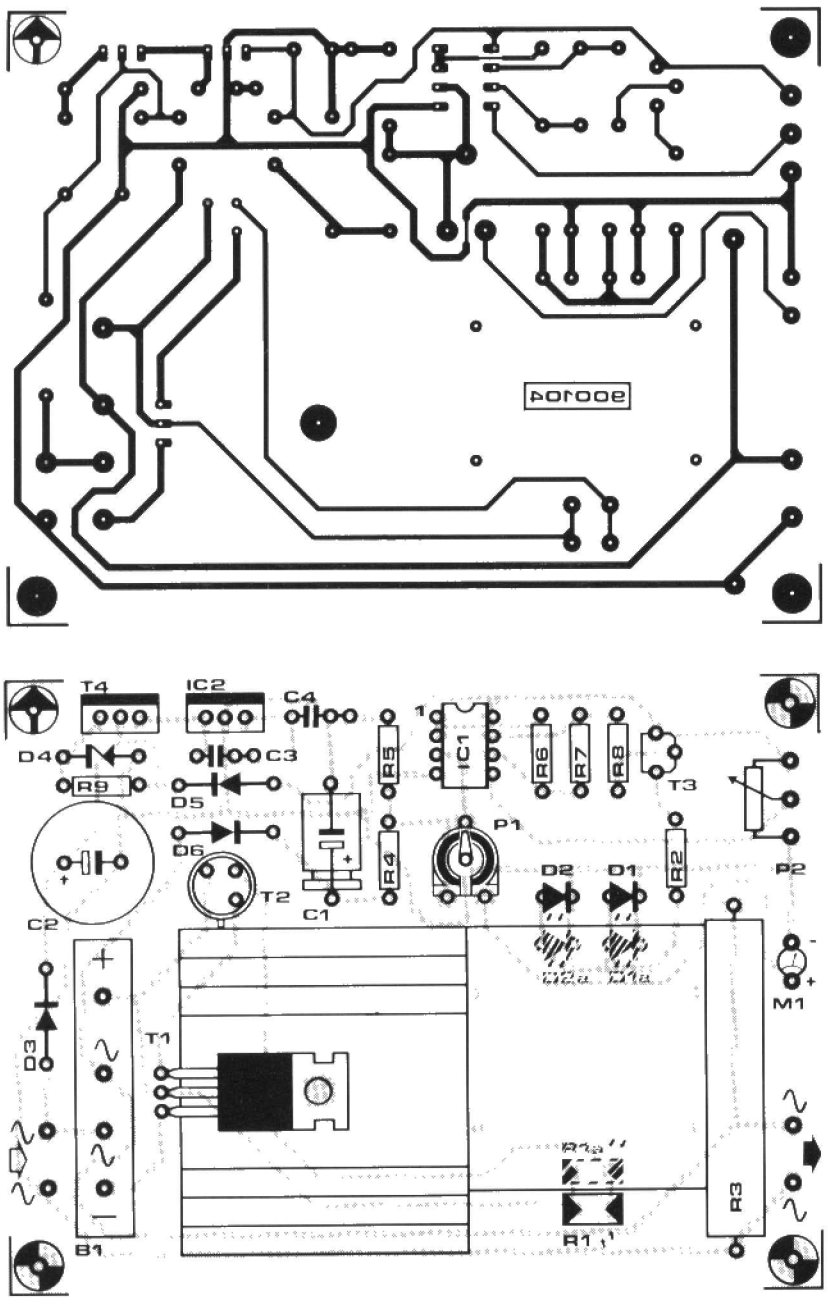


Fig. 4. Single-sided printed circuit board for the a.c. power supply.

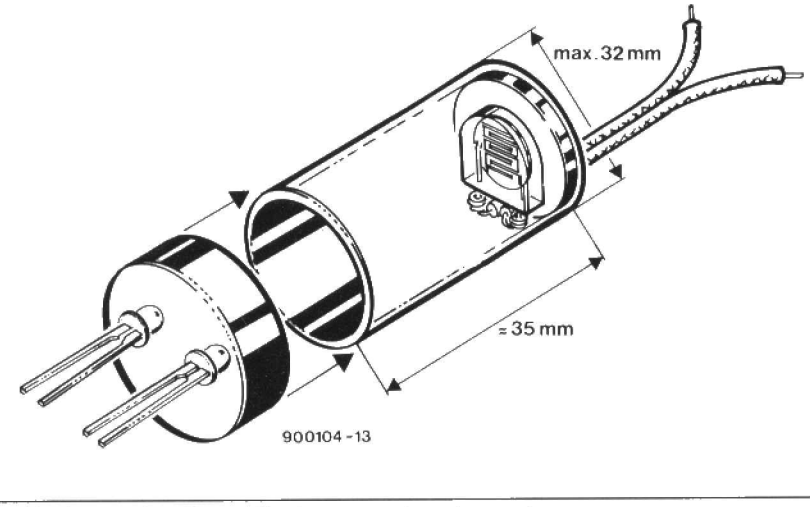


Fig. 5. Basic construction of the home-made optocoupler.

COMPONENTS LIST

Resistors:

1	LDR	R1
1	180Ω	R2
1	100Ω 10W	R3
1	47kΩ	R4
1	39kΩ	R5
2	100kΩ	R6;R7
1	22kΩ	R8
1	220Ω	R9
1	1MΩ preset H	P1
1	2kΩ2 lin. potentiometer	P2

Capacitors:

1	10µF 63V axial	C1
1	220µF 50V radial	C2
1	330nF	C3
1	10nF	C4

Semiconductors:

2	red LED	D1;D2
3	1N4001	D3;D5;D6
1	33V 0.4W zener diode	D4
1	B80C3200/2200	B1
2	BD241	T1;T4
1	BC141	T2
1	BC550B	T3
1	TLC272	IC1
1	7812	IC2

Miscellaneous:

1	double-pole mains switch	S1
1	mains appliance socket with integral fuseholder	K1
1	mains transformer 30V @1A, e.g., ILP 11013 (220V mains) or ILP 13013 (240V mains)	Tr1
1	100µA moving-coil meter	M1
1	160mA fuse (slow)	
1	heat-sink for T1; 7K/W	
2	heat-sink for T4 and IC2; 30K/W	
1	printed-circuit board	900104
1	front-panel foil	900104-F
1	enclosure LC850 (manufacturer: Telet; supplier: C-I Electronics)	

Opamp IC1a buffers the voltage supplied by R4-R5, and drives IC1b, the difference amplifier proper. Potentiometer P2 forms the output voltage control. The voltage at its wiper is compared with the voltage supplied by IC1a. The error voltage supplied by IC1b is buffered by T3, and used to control the intensity of two parallel-connected LEDs in an optocoupler. The LDR (light-dependent resistor) at the other side of the optocoupler determines the resistance formed by T1.

Unfortunately, the power supply has some shortcomings because of the use of a power transistor as an adjustable resistor in the regulating circuit. For one thing, the resistance can not become nought since T1 will introduce a minimum drop of about 2.5 V. Add that to the drop across the diodes, and you will realize that the total voltage loss introduced by the regulator is about 4 V. Similarly, T1 can never be turned off completely.

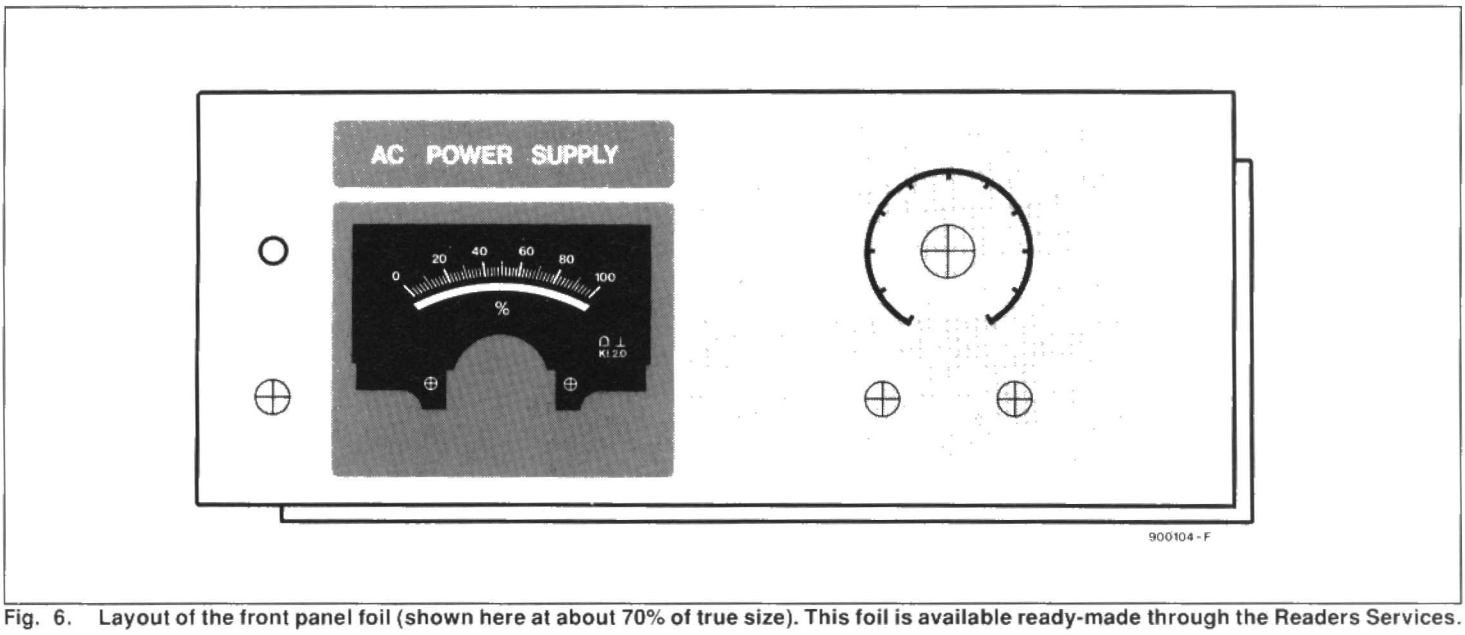


Fig. 6. Layout of the front panel foil (shown here at about 70% of true size). This foil is available ready-made through the Readers Services.

This means that the supply can not be set to an output voltage of 0 V. Fortunately, the actual minimum output voltage is quite low at a value smaller than 0.5 V.

The regulation circuit is powered by the mains transformer via rectifier D3-C2. Components R9, D4 and T4 reduce the rectified voltage to about 33 V, which can then be safely applied to the input of a 12-V regulator, IC2.

Construction

The construction of the power supply is straightforward if you use the printed-circuit board shown in Fig. 4. The optocoupler is a home-made device. The construction is shown in Fig. 5. Use a length of PVC tubing, a (black) spool of a photographic film, or cut a piece of thin, black decoration cardboard to size and roll it into a tube.

The printed-circuit board enables the LDR and the LEDs to be connected in two ways, allowing you to determine where the respective component terminals exit from the optocoupler assembly.

The heat-sinks of T4 and IC2 need not be large — in most cases, two pieces of aluminium of an area of about 15 mm^2 will do. Make sure that the heat-sinks do not touch. Alternatively, IC2 and T4 may be mounted on a common heat-sink, provided both components are fitted with insulating washers.

The power supply is housed in a metal enclosure Type LC850 from Telet. The dimensions of the blue-and-grey self-adhesive front-panel foil for the supply (Fig. 6) are geared to this type of enclosure..

The two toroid transformers stated in the components list have two 15-V secondary windings, which must be connected in series to obtain the required 30 V.

The power supply has only one adjustment. Connect an a.c. voltmeter to the supply and set an output voltage of 25 V. Next, adjust P1 until the moving-coil meter indicates the same value. ■

CORRECTIONS

6-metre band converter

April 1991, p. 38-43

The components list and the inductor overview in the top left hand corner of the circuit diagram should be corrected to read:

L1, L2 = 301KN0800.

Capacitor C16 (4.7 pF) must not be fitted on the board.

Finally, a few constructional tips:

- Fit a 10 nF ceramic decoupling capacitor at junction L7-R36.
- Fit a 18 kΩ resistor between the base of T3 and ground. This reduces the Q factor of L2, and prevents too high signal levels at the base of T3.
- For improved tuning, inductor L9 may be replaced by a Toko Type 113KN2K1026HM.

Multifunction measurement card for PCs

January and February 1991

We understand that the 79L08 (IC17) is no longer manufactured and, therefore, difficult to obtain. Here, the IC may be replaced by a 7908, which, although physically larger than the 79L08, is pin-compatible, and should fit on the PCB.

Dimmer for halogen lights

April 1991, p. 54-58

In the circuit diagram of the transmitter, Fig. 2, pin 14 of the MV500 should be shown connected to pin 13, not to junction R1-R2-C2. The relevant printed-circuit board (Fig. 6) is all right.

RDS decoder

February 1991, p. 59

Line A0 between the 80C32 control board and the LC display is not used to reset the display, but to select between registers and data.

We understand that the SAF7579T and the associated 4.332 MHz quartz crystal are difficult to obtain through Philips Components distributors. These parts are available from C-I Electronics, P.O. Box 22089, 6360 AB Nuth, Holland. For prices and ordering information see C-I's advertisement on page 6 of the May 1991 issue.

S-VHS-to-RGB converter

October 1990, p. 35-40

Relays Re1 and Re2 must be types with a coil voltage of 5 V, not 12 V as indicated in the components list. Constructors who have already used 12-V relays may connect the coils in parallel rather than in series.

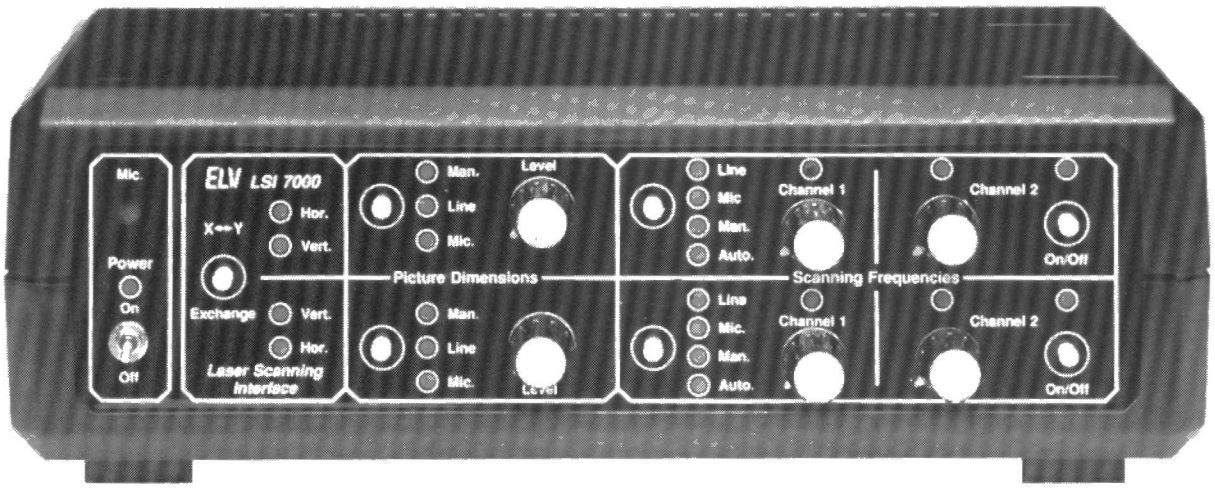
Suitable 5-V relays for this project are the 3573-1231.051 from Günther, and the V23100-V4305-C000 from Siemens.

The components list should me modified to read:

6 33nF C57-C62

LASER

PART 2: CONTROL UNIT LSI7000 (CIRCUIT DESCRIPTIONS)



Following last month's description of the laser exciter and the mirror galvanometer assembly we now turn to a state-of-the art electronic control unit for the show laser.

Continued from the May 1991 issue.

The laser control unit described here is a fairly complex design capable of producing attractive laser patterns. The complete control unit contains some 250 resistors, 100 capacitors and 40 integrated circuits. Fortunately, the assembly of the kit is pretty easy, although it will require several hours of careful soldering work. More about this next month, though, as the present instalment deals mainly with circuit descriptions.

Pretty sine-waves

Many of you will be familiar with Lissajous patterns on an oscilloscope. Being rather static, Lissajous patterns would appear to be less suitable as show effects for a laser as discussed here. Bear in mind, however, that an oscilloscope produces such patterns when fed with two fixed signals only. A first step towards the creation of moving Lissajous patterns is simply to replace one of the fixed signals by a music signal (or, more generally, an audio signal). The result is a pretty erratic type of pattern on the scope. Some static patterns can be interesting, too, and are simple to produce by increasing the number of sine-waves. The present laser control unit supplies four sine-waves that allow a wide variety of patterns to be created.

The block diagram in Fig. 8 is fairly complex, and indicative of the number of components used to build the laser control unit. The output of the circuit is formed by two 1-watt a.f. power stages that drive the coils in the mirror galvanometers. An electronic double-pole changeover switch fitted ahead of the power output stages allows you to swap the drive signals produced by the two audio interface channels, left and right.

Since the right and left channels are virtually identical, the circuit description will refer to one channel only, in this case, the left one. The input signals for the power output stages are supplied by an electronic potentiometer that allows you to control, independently, the signal frequency (i.e., the shape of the pattern) and the signal amplitude (i.e., the size of the pattern).

There are three sources for the amplitude control signal, which is selected via electronic switches. When the constant voltage source is selected, you can control the size of the pattern via the LEVEL potentiometer. The level information is obtained from an envelope detector when the LINE, LS (loudspeaker) or microphone signal is selected. The LEVEL potentiometer then enables you to set the maximum pattern size reached at a certain level of the input signal.

The LINE, LS and microphone signals may be used to create the laser patterns. In addition to these sources, two sine-wave generators are available of which the output frequency can be set manually as well as by means of a timer circuit. Before these signals are applied to the electronic potentiometer, they are taken through a frequency compensation circuit that serves to correct the frequency response of the mirror galvanometers. Additionally, the audio signals are taken through a 150-Hz low-pass filter that suppresses signal components that can not be reproduced anyway.

The audio signal may be supplied by the microphone contained in the laser control unit. This microphone is used to drive both channels via a compressor circuit that ensures a fairly constant drive level. The same goes for the LINE and LS signals, which are also taken through a compressor. The difference between the LINE and the LS input is mainly the required signal level. The LINE inputs accept relatively small signals (line level), while the LS inputs can be driven with higher voltages as supplied, for instance, by the loudspeaker output of an a.f. power amplifier.

Two sine-wave generators are available on each channel of the laser control unit. A switch, marked CHANNEL 2 ON/OFF, is used to select one sine-wave or the sum signal of two sine-waves. The frequency of these is determined by applying a control voltage to the generators. The control voltages can be set manually or by means of a generator that supplies a slow triangular voltage. The

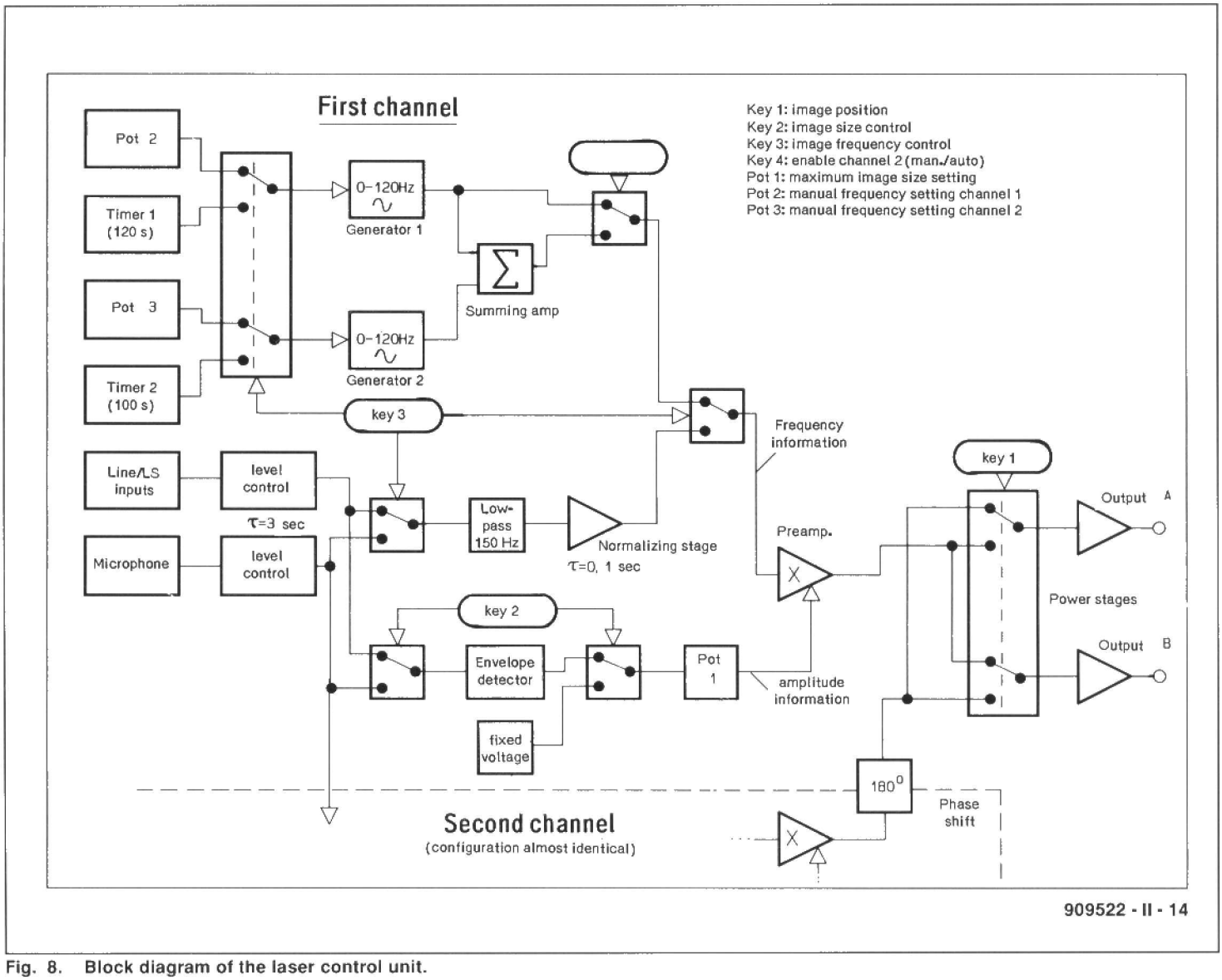


Fig. 8. Block diagram of the laser control unit.

period time of the triangle is about 100 s, but the actual value is slightly different for each of the four generators in the control unit. The differences are such that it takes more than 24 hours (theoretically) before the same pattern is repeated.

Circuit diagram

The circuit diagram, Fig. 9, of the laser control unit follows the block diagram quite closely. For the sake of simplicity a few blocks are drawn in Fig. 2 that contain circuits discussed in detail further on.

The LINE and LS signals are applied to the circuit via sockets Bu1 to Bu4, which are connected via a potential divider for the right and left channel. This means that the LS socket and the LINE socket next to it can not be used simultaneously. Fortunately, the high impedance of the potential divider prevents damage to equipment when the LS and LINE inputs are accidentally used at the same time. The input signals are first fed to a compressor, whose operation is discussed further on.

The microphone is a small electret type with a built-in FET amplifier. It is connected to terminals ST1, ST2 and ST3. The microphone signal is amplified by IC1 before it is applied to the compressor. The three compressors are followed by the input selection switches that enable the signals to be routed in one of two directions: to the frequency-determining circuits, or to the amplitude-determining circuits.

In the frequency-determining branch, the signal is first applied to a 150-Hz filter set up around T1 (T3 for the right channel). Then follows another switch, this time for the selection between the audio source and the generator. After the frequency compensation the signal arrives at electronic potentiometer IC4.

In the amplitude-determining branch the audio signal is fed to T2 and T4, which form an envelope detector. The switch contact that follows the detector allows the size of the patterns to be controlled manually or by the envelope waveform of the audio signal. The latter function requires a constant voltage, which is obtained from a regulated supply voltage with the aid of a potential divider. The amplitude control signal is subsequently amplified to allow the final size of the laser pattern to be set by the LEVEL control, R26-R40. Next, the level information is applied to the control inputs of an electronic potentiometer, IC4. The output signal of IC4 is buffered by IC2b and IC3b before it arrives at the switch contacts that allow you to determine the channel assignment (left/right; L/R) for the horizonal and vertical (H/V) deflection of the laser beam. From the poles of the H/V-L/R switches the signal is taken to the inputs of the two power amplifiers that drive the mirror galvanometers.

The generators

There are two almost identical generators in the laser control unit. The difference between them is the value of a single resistor. Figure 10 shows the circuit diagram of the generator for the left channel. All components are numbered from 100 onwards. For the right channel, the corresponding components are identified as 2xx. Note, however, that resistor R62 in the left channel appears as R64 in the right channel.

The heart of the generator is formed by two integrated circuits Type XR2206, a well-known function generator from Exar. The frequency of the output sine-wave produced by the generator is determined by a control voltage obtained either from potentiometer R141-R147 via an amplifier, or from a generator.

The circuit for the automatic frequency control of the sine-wave generator may look

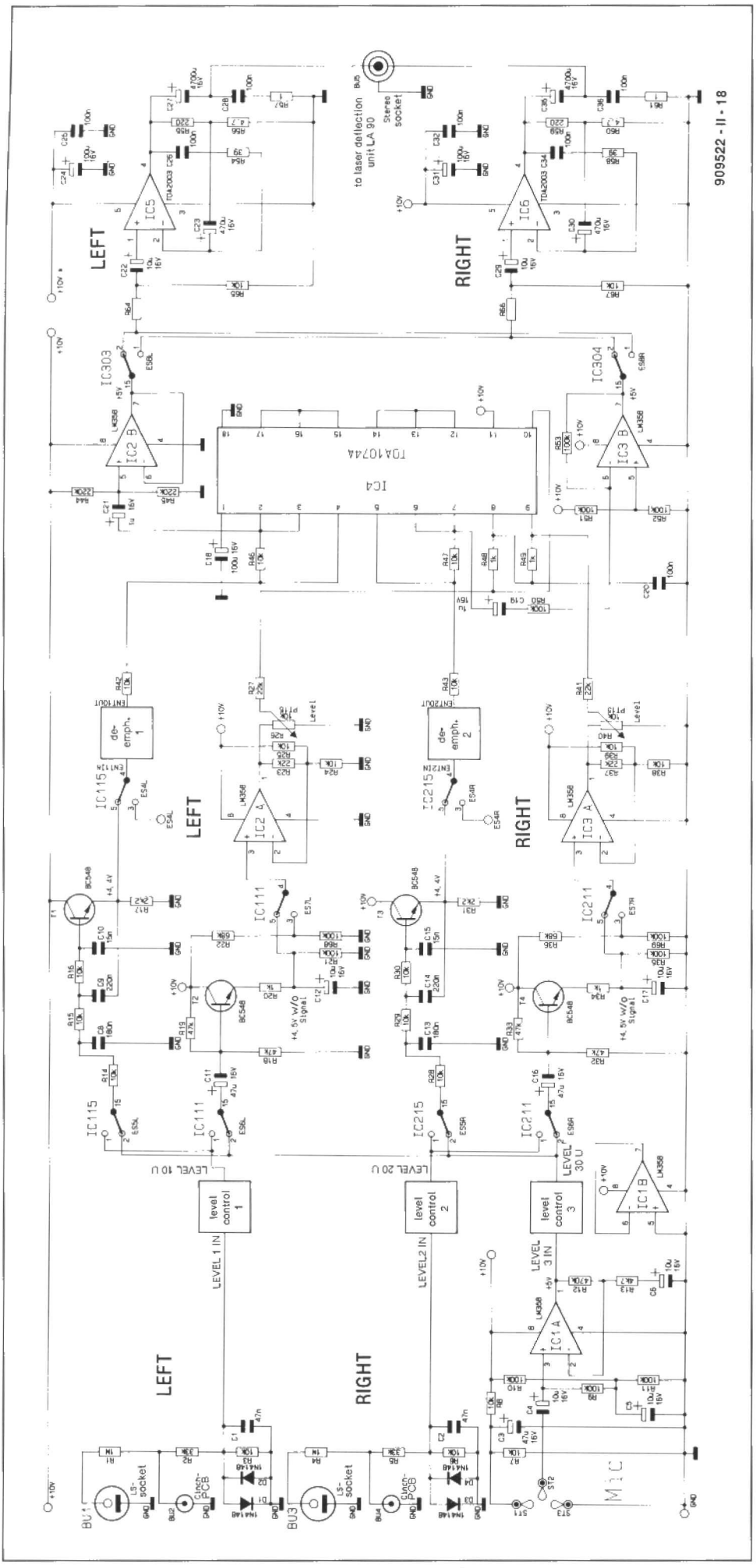


Fig. 9. Main circuit diagram of the laser control unit. Some circuit sections are shown as modules here.

unusual at a first glance. Fortunately, it operates in a rather simple way. Opamps IC103a and IC103b form two Schmitt-triggers set up as square-wave generators. Concentrating on IC103a for the moment, we see that the opamp is wired to function as a Schmitt-trigger by means of resistors R137, R138 and R139. The Schmitt-trigger is turned into a square-wave generator by components R140 and C119. A square wave is, however, not what we are after if we want the sine-wave generator to produce a continuous frequency range. Fortunately, the capacitor, C119, has on it a triangular waveform that does allow a true, linear, VCO (voltage-controlled oscillator) function to be realized. The capacitor voltage, which is a triangular waveform with a period time of about 100 s, is buffered by opamps IC103c and IC103d. Note that the period time is chosen slightly differently for the other generator. This is done to prevent the laser repeating the same pattern after 100 s when the 'automatic' mode is used. The differently set period times ensure that it takes at least 24 hours before a pattern is repeated (this is based on the assumption that component tolerances have no effect).

The generator circuit is followed by a summing amplifier, IC107, that serves to add the two sine-waves. Electronic switch IC115 allows you to select either the output signal of IC105 only, or the mixed output of the two sine-wave generators.

The compressor

The circuit diagram of the compressor is shown in Fig. 11. The component numbers refer to the left channel — the circuit of the right channel compressor is identical, with component numbers in the '200' range. The component numbers in the microphone compressor start at 300.

Opamp IC101b supplies a stable and adequately decoupled reference voltage to the circuit. The a.f. input signal is applied to the compressor via capacitor C101. Opamp IC101a forms an amplifier whose gain is determined by FET T101, which functions as a voltage-controlled resistance. The output signal level of IC101a is monitored with the aid of a further opamp, IC101d, whose output is connected to a rectifier, D101-D102-C104. To close the a.f. level control loop in the compressor, the direct voltage supplied by the rectifier is fed to the gate of FET T101. The gate voltage determines the a.c. resistance of the drain-source junction, and thus the gain of IC101a. The compressor has an inverse level control characteristic, which means that its gain is reduced as the input signal level increases. In this manner, the compressor ensures that the mirror driver circuits are provided with a reasonably constant input signal.

Frequency compensation

As discussed last month, the deflection of the mirror galvanometers is frequency dependent, i.e., not linear. To linearize the response, a frequency compensation circuit is used —

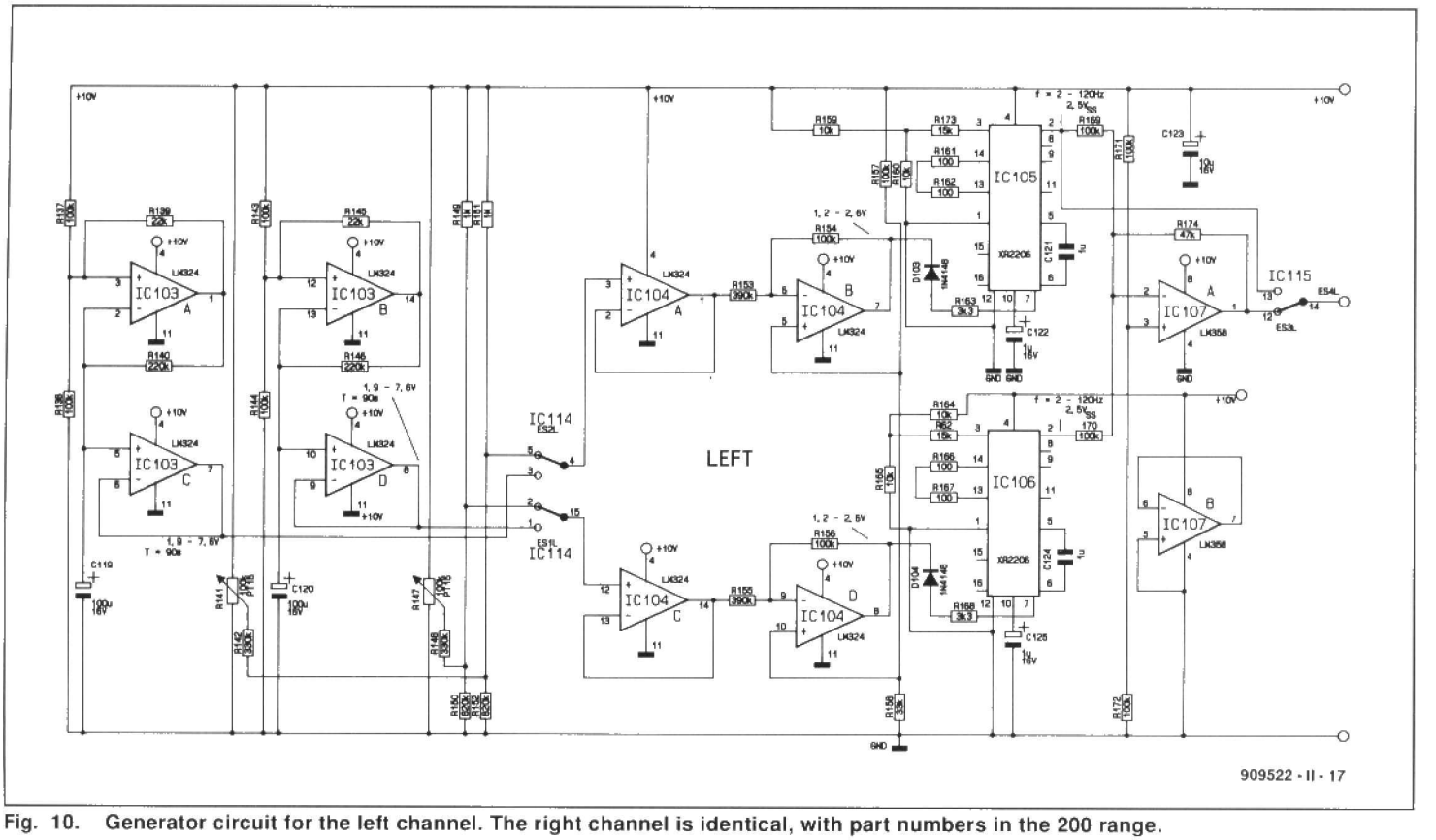


Fig. 10. Generator circuit for the left channel. The right channel is identical, with part numbers in the 200 range.

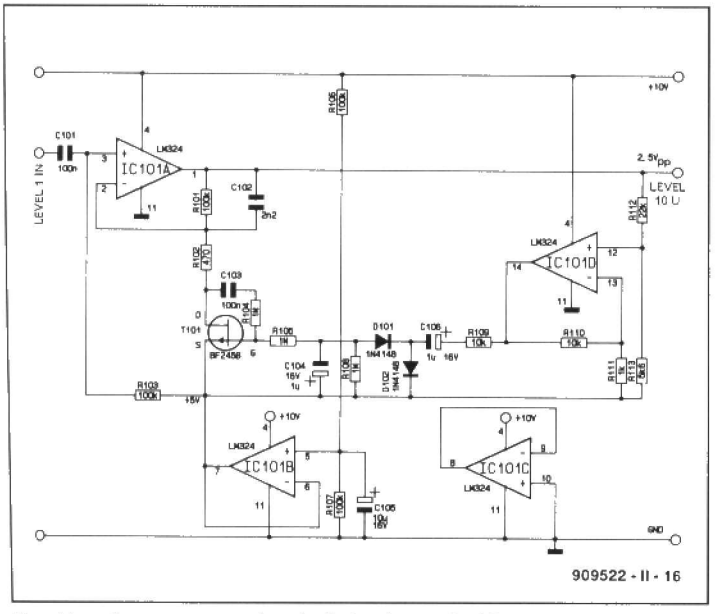


Fig. 11. Compressor circuit (left channel). The component numbers for the (identical) right channel are in the 200 range, and those for the microphone channel in the 300 range.

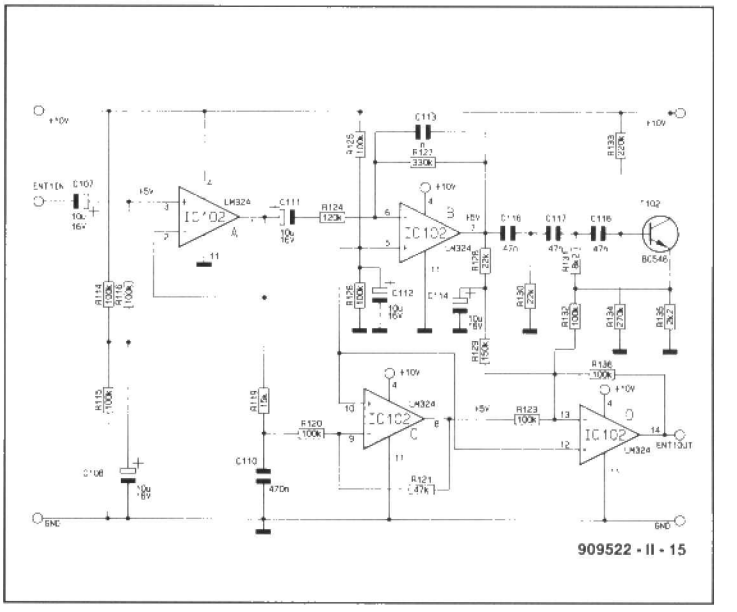


Fig. 12. Frequency compensation circuit for the mirror galvanometer driver in the left channel. A number of filters are used to linearize the frequency response of the mirror over a small range.

see Fig. 12. The circuit starts with a buffer, IC102a, and ends with a summing amplifier, IC102d. The latter adds the signals supplied by a number of filter sections in the circuit via resistors R123, R129 and R132. A filter based on T102 provides a rising filter slope from 50 Hz onwards. The falling slope of the filter response is set to start at about 200 Hz with the aid of R127 and C113. Returning to the low end of the filter response, components R119-C110 create a falling slope from 15 Hz onwards, i.e., before the rising part which starts at 50 Hz. The last filter section, R128-C114, serves to correct the filter response for frequencies below 15 Hz.

The result of all this filtering and summing is a virtually linear response of the mirror galvanometers, i.e., their deflection is independent of the signal frequency when the signal level is held constant.

Next time

The above descriptions cover most of the operation of the laser and the associated control unit. In next month's final instalment we will complete the description by discussing the way in which the electronic switches are controlled. The article will be closed with a description of the way in which the laser control unit is built and operated. ❑

LIGHT SWITCH WITH TV REMOTE CONTROL

Why not use the infra-red remote control, that magic little box supplied with every TV set these days, for applications other than channel hopping and turning the volume up when your favourite pop group appears on the screen? The simple IR receiver discussed here responds to most types of TV remote controls, and can be used to switch lights and other appliances on and off.

J. Ruffell, from an idea by M. Dupessey

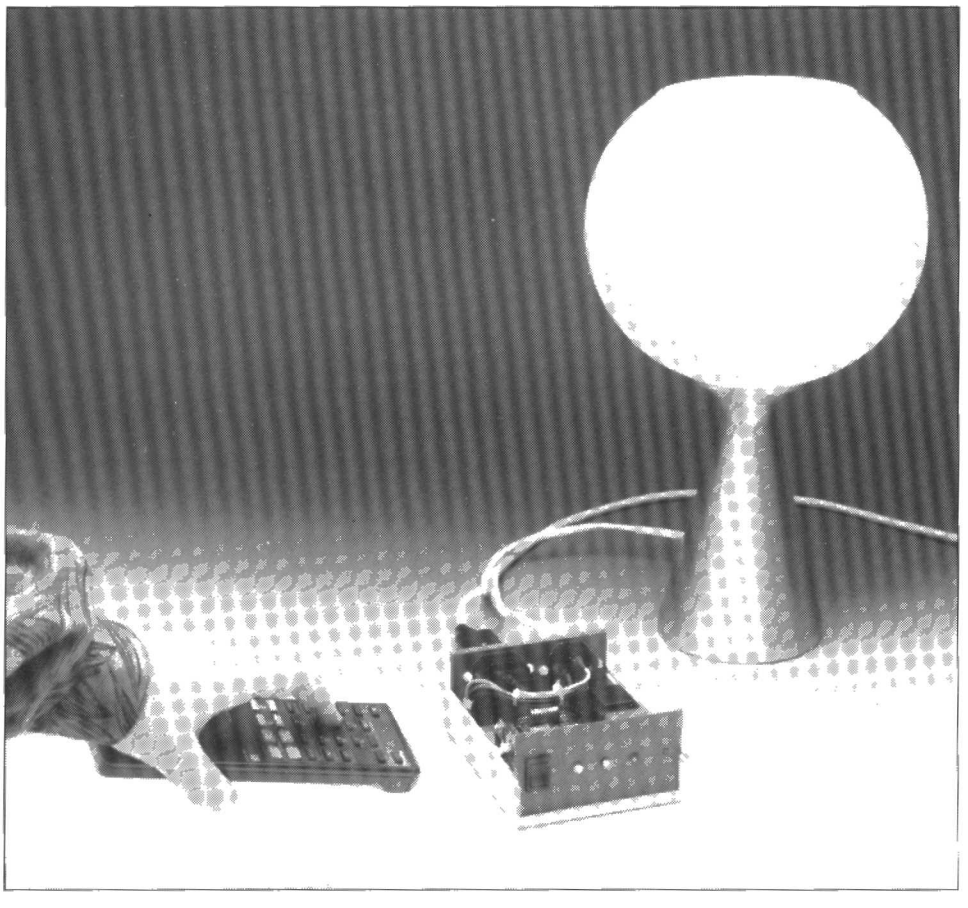
PRACTICALLY all TV sets these days are supplied with an infra-red remote control. Provided they have not been dropped too often, or chewed on by our beloved pets (we mean domestic animals including parrots and budgerigars), these handy little boxes allow us to remain comfortably seated in front of the 'tube' and exercise total control over the channel selection and a plethora of other settings of the TV set.

As shown in this article, it is perfectly possible to use a remote control box for an application not foreseen by the manufacturer. The general idea is illustrated in Fig. 1: here, the IR remote control is used to switch a light on and off. In some cases, it is even possible to switch the TV set on and off as well, although this requires a small change in the receiver. Note, however, that many modern TV sets already have a standby/active function controlled via the IR box.

Single-chip IR receiver

The IR receiver is based on an integrated circuit Type TDE4061 from Siemens. The internal diagram of the chip is given in Fig. 3. The main technical characteristics are:

- Low stand-by current: 650 µA;
- Supply voltage range: 4 V to 6.5 V;
- Frequency range up to 200 kHz
- Available with and without demodulator output (TDE4061/TDE4060);
- No inductor required in external circuit;
- High ambient light rejection;
- Bipolar technology couples good high-frequency behaviour with a low current consumption;
- Suitable for battery supply.



The input of the TDE4061 (see Fig. 3) is connected to an infra-red photodiode, which unfortunately not only 'sees' the signal from the IR remote control box, but also visible light, 100-Hz interference from incandescent bulbs, and a part of the light spectrum emitted by fluorescent tubes.

The input stage is followed by a bandpass filter that serves to extract the IR remote control signals from the interference. The demodulator block drawn in Fig. 3 is not available in the TDE4060.

A current sink circuit is provided to suppress low-frequency currents supplied by the photodiode, and stabilize the bias at the input of the IR preamplifier at 1.4 V. The gain of the preamplifier is automatically controlled to ensure optimum drive of the bandpass filter.

The IFR (infra-red) input of the TDE4061 forms a high impedance, and is suitable for input currents in the nano-ampere range. Hence, the anode of the photodiode is connected direct to the IFR input.

The output of the TDE4061, Q, supplies a demodulated digital signal. An example of an output signal is shown in Fig. 2 for the Aristona (Philips) remote control Type RC4520. Note that the pulse lengths, T1 to T4, shown in the diagram depend on the IR remote control used.

Circuit description

As shown in Fig. 4, very little is required to build an IR receiver based on the TDE4061. In the following description, some points will be noted that may be of interest to those of you who want to use the TDE4061 for their own applications.

The IR photodiode, D3, is a Type BPW41N from Telefunken. It is forward biased via resistor R5, and supplies a photocurrent to the IFR input of the TDE4061.

Capacitor C1 and resistor R5 form a low-pass filter at the IFR input that serves to suppress interference. The capacitor at the C_{REG} input of the TDE4061, C5, determines the time constant of the preamplifier. The value of this capacitor is set to 470 nF to suit the bi-phase-coded signals emitted by most modern IR remote controls. The capacitor must be made smaller when an IR system is used that does not supply run-in signals for the gain control circuit of the receiver. In these cases, C5 may be reduced to about 10 nF. Do not go lower than this value to prevent oscillation.

The capacitor at the CS input of the TDE4061, C7, gives the preamplifier a high-pass characteristic, and works in conjunction with G_{REG}, and the double-T network at the RC1 and RC2 connections of the IC. These components determine the settling behaviour of the TDE4061 following fast signal changes. The CS capacitor tunes the receiver to the carrier emitted by the IR remote control. Depending on the carrier frequency, C7 is 100 nF (for 30 kHz systems) or 10 nF (for 120 kHz systems).

The bandpass filter that follows the IR preamplifier improves the signal-to-noise ratio of the IR signal and reduces the jitter on the digital output signal. The external double-T *R*-*C* bandpass filter connected to the RC1 and RC2 pins of the TDE4061 must provide a d.c. path, and have a band-stop (notch) characteristic. The notch frequency, f_c, is made equal to the IR carrier frequency. It is given by

$$f_c = 1/(RC) \qquad [Hz]$$

where R=R6=R7, and C=C9=C2. Note that R8=$R/2$, and C8=2C. To keep the voltage drop across the filter within reason, R must not be made larger than 100 kΩ. The values

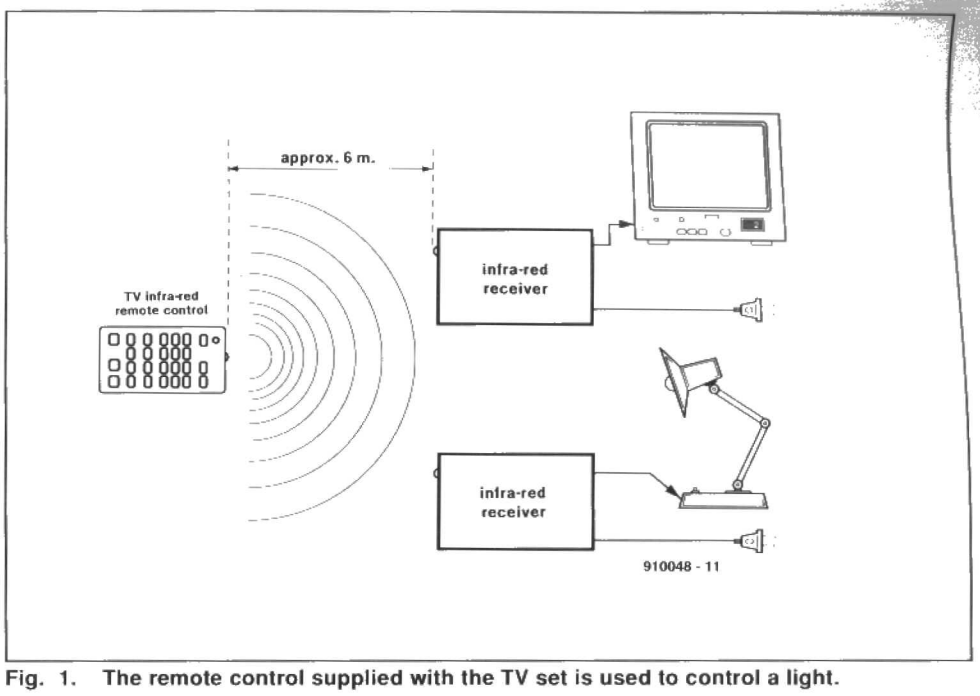


Fig. 1. The remote control supplied with the TV set is used to control a light.

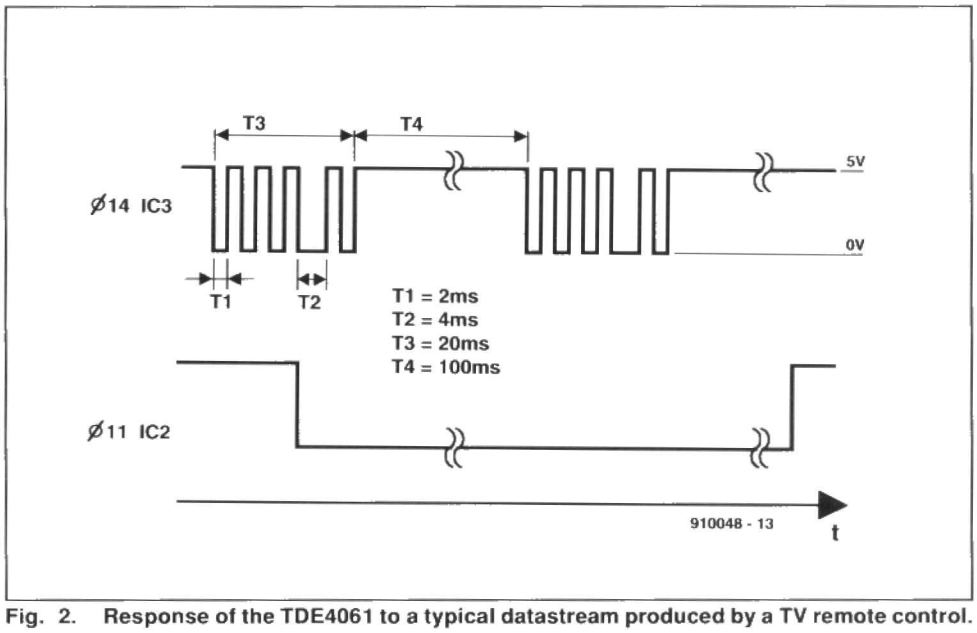


Fig. 2. Response of the TDE4061 to a typical datastream produced by a TV remote control.

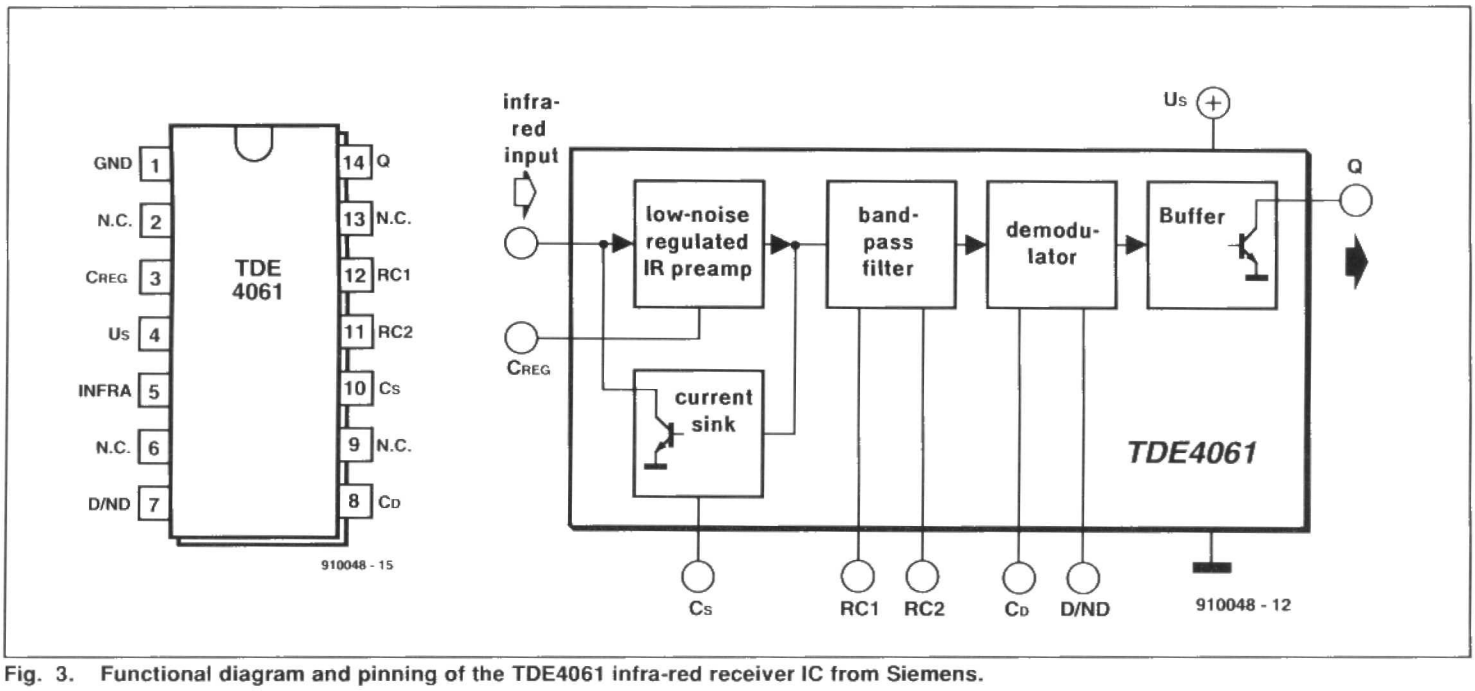


Fig. 3. Functional diagram and pinning of the TDE4061 infra-red receiver IC from Siemens.

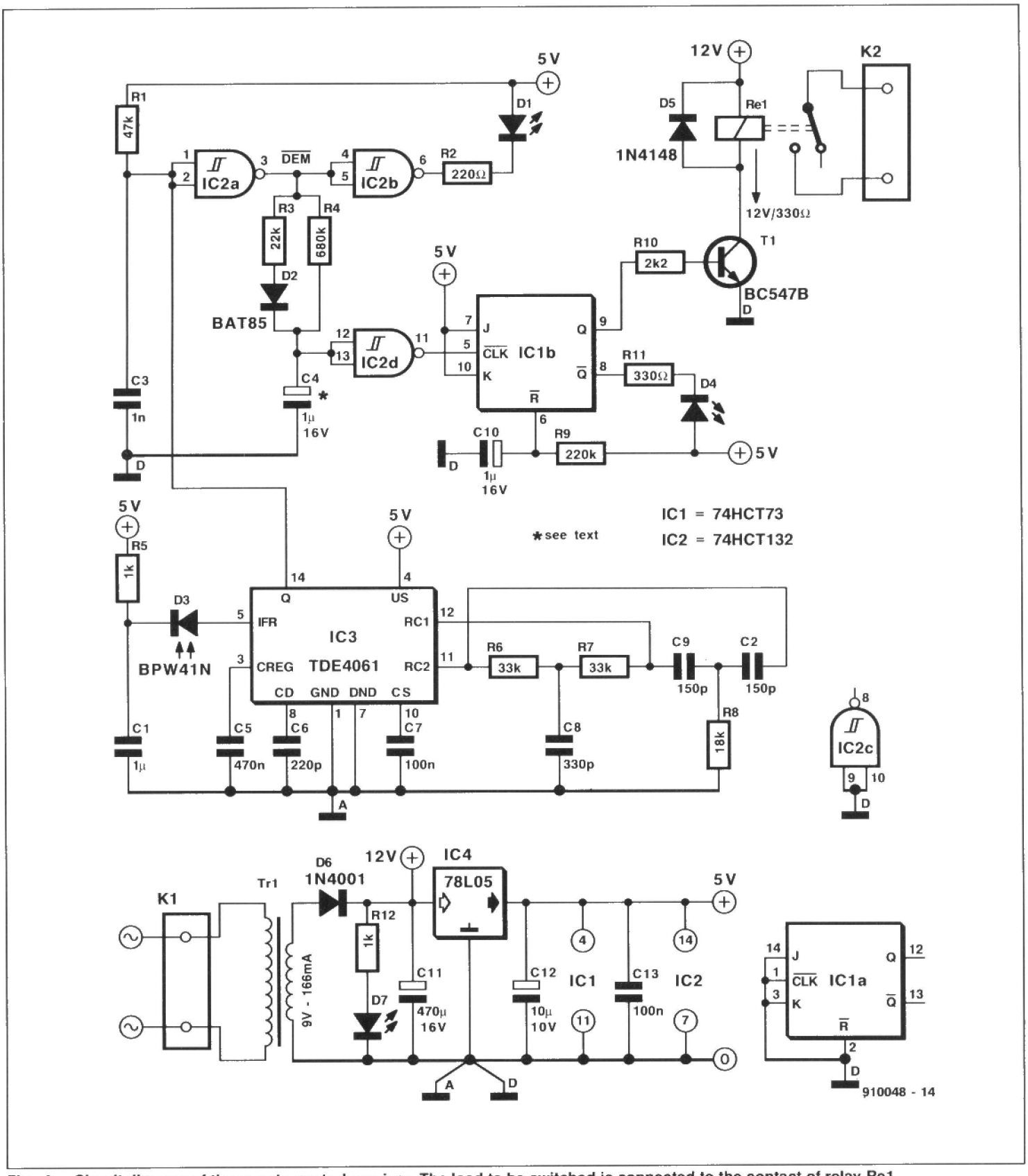


Fig. 4. Circuit diagram of the remote control receiver. The load to be switched is connected to the contact of relay Re1.

of the external filter components may have to be changed experimentally to suit the previously mentioned pulse lengths supplied by the IR remote control.

The output of the TDE4061, Q, is of the open-collector type. When the output transistor is switched on, the maximum collector current is 1 mA. In designs where the output signal is fed back to the input, oscillation may occur if the output current is not kept smaller than about 200 µA. Note that this type of feedback is not applied in the present circuit.

The digital pulse train supplied by the TDE4061 is inverted by a Schmitt-trigger gate, IC_{2a}, and subsequently rectified by D_2-C_4 to obtain an on/off control signal. Every trailing edge of the switching signal supplied by IC_{2d} causes J-K bistable IC_{1b} to toggle, so that the relay, Re_1, is actuated or de-actuated. This creates a simple on/off toggle function.

The load controlled via the IR system is connected to the contact of Re_1. LED D_1 lights in the rhythm of the pulses when an IR signal is received. When the Q output of IC_{1b} is logic high, transistor T_1 conducts, and the relay is actuated. The complementary output, $\overline{Q}$, of the bistable is then low, and LED D_4 lights to indicate the relay status.

The response of the receiver to IR control signals is determined by the value of C_4. This capacitor effectively turns the pulse train

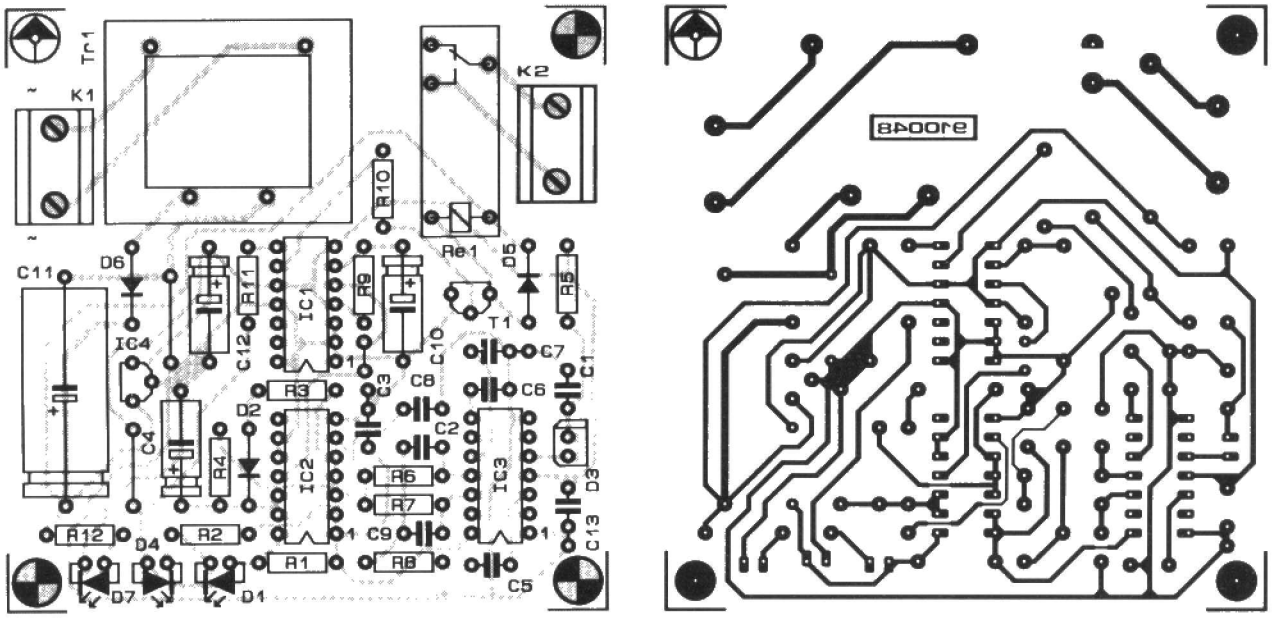


Fig. 5. Single-sided printed circuit board for the IR remote control receiver.

COMPONENTS LIST

Resistors:

1	47kΩ	R1
1	220Ω	R2
1	22kΩ	R3
1	680kΩ	R4
2	1kΩ	R5;R12
2	33kΩ	R6;R7
1	18kΩ	R8
1	220kΩ	R9
1	2kΩ2	R10
1	330Ω	R11

Capacitors:

1	1µF solid	C1
2	150pF	C2;C9
1	1nF	C3
1	1µF 16V (see text)	C4
1	470nF	C5
1	220pF	C6
2	100nF	C7;C13
1	330pF	C8
1	1µF 16V	C10
1	470µF 16V	C11
1	10µF 10V	C12

Semiconductors:

1	green LED dia. 3mm	D1
1	BAT85	D2
1	BPW41N (Telefunken)	D3
1	yellow LED dia. 3mm	D4
1	1N4148	D5
1	1N4001	D6
1	red LED dia. 3mm	D7
1	BC547B	T1
1	74HCT73	IC1
1	74HCT132	IC2
1	TDE4061 (Siemens)	IC3
1	78L05	IC4

Miscellaneous:

1	3-way 5mm pitch PCB terminal block	K1
1	2-way 5mm pitch PCB terminal block	K2
1	12V/330Ω PCB mount relay, e.g., Siemens V23127-B2-A101	Re1
1	9V/166mA PCB-mount mains transformer, e.g., Monarch VTR-1109/IV	Tr1
1	Printed circuit board	910048

into an on/off pulse with a much longer period. This is achieved by a relatively small resistor and a diode, R3-D2, through which the capacitor charges, and a relatively large resistor, R4, through which the capacitor discharges.

The receiver is completed by a standard 5-V regulated supply based on an 78L05, IC4.

Construction

The IR receiver is a compact unit because all components are fitted on a single printed-circuit board, which is shown in Fig. 5. Start the construction by fitting the three wire links on the board. Next, fit the resistors, the diodes, the capacitors, and the active components. Use sockets for the ICs, which are not plugged in until the board is completely assembled.

Complete the construction of the board by mounting the transformer, the relay and the soldering pins. The three LEDs are fitted such that their faces protrude from holes in the plastic enclosure. The infra-red diode, D3, is fitted on the front panel of the case. It is secured such that its light-sensitive area can 'see' the remote control. The light-sensitive area of the BPW41N is located at the centre of the flat front side of the device.

After finishing the construction of the PCB, connect the mains cable to K1, a 3-way PCB mount terminal block of which the centre pin is cut off. Next, connect the load to K2.

To enable you to experiment with different values, the PCB allows capacitors with two different lead spacings to be fitted in positions C3, C7 and C13.

Practical use

With most remote control boxes the usable range of the receiver will be greater than 5 metres. Since the response time of the receiver is relatively short at a few tens of milliseconds, the unit must be installed at some distance from the TV set to prevent it being triggered by control commands intended for the TV set. If you still want to locate the receiver close to the TV set, increase the value of C4 to, say, 47 µF. This results in a much longer response time to remote control commands. ■

APPLICATION NOTES

The contents of this article are based on information obtained from manufacturers in the electrical and electronics industry and do not imply practical experience by *Elektor Electronics* or its consultants.

UHF AUDIO/VIDEO MODULATOR TDA5664X (Siemens Components)

THE new TDA5664X from Siemens Components is an integrated circuit that contains all functions required to mix and modulate video and audio signals at frequencies between 30 MHz and 860 MHz. The new TV modulator IC is intended for use in video recorders, cable network converters, video pattern generators, closed-circuit TV systems, amateur TV transmitters and personal computers.

The advantages of the TDA5664X over its predecessor, the TDA5660P, are:

- 5-V supply voltage;
- no circuit adjustment required;
- reduced external circuit;
- smaller package (DIP14);
- also available in SMA package (SO14);

In addition to these advantages, the TDA5664X has the following specific features:

- FM sound modulation;
- sync-pulse clamping circuit at video input;
- clipping at peak white level;
- continuously adjustable modulation depth for positive and negative video modulation;
- high residual carrier suppression;
- low spurious radiation.

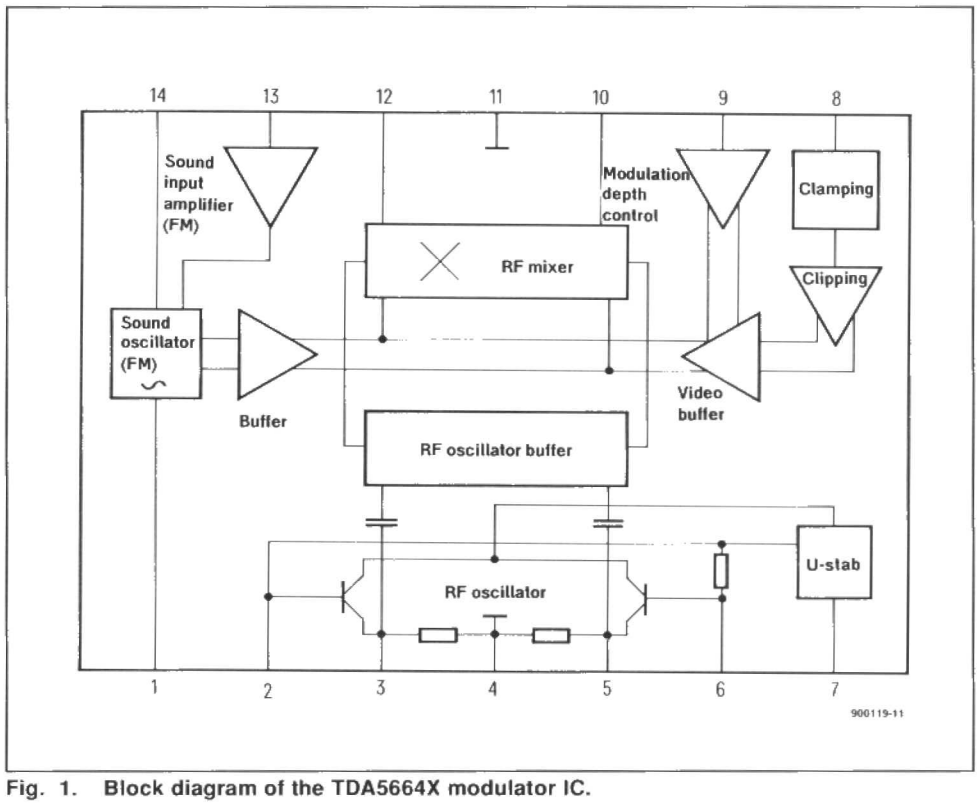


Fig. 1. Block diagram of the TDA5664X modulator IC.

Block diagram

The composite video signal with negative-going synchroniaztion pulses is applied to pin 8 via a coupling capacitor (see Fig. 1). The on-chip clamping circuit fixes the video signal level relative to the synchroniaztion pulses. When the video signal exceeds 1 V, the peak white level is clipped. Negative AM video signal modulation is selected by leaving pin 9 of the IC non-connected. When pin 9 is connected to ground, the RF carrier is positively modulated. If desired, a variable resistor may be connected between pin 9 and ground to enable the modulation depth to be controlled.

The TDA5664X is capable of modulating video as well as sound. The audio signal is capacitively coupled to the AF input of the IC, pin 13. A pre-emphasis network may be connected externally. The output signal of the audio input amplifier is frequency-modulated on to a 6.0 MHz (UK) or 5.5 MHz subcarrier. The output signal of the subcarrier oscillator is mixed with the output signal of an on-board RF oscillator. The operating frequency of the sound subcarrier oscillator is determined by an external *L*-*C* parallel tuned circuit connected between IC pins 1 and 14. This tuned circuit may be damped by an external resistor, R5, to set the sound subcarrier amplitude with respect to the vision carrier amplitude.

The amplifier that forms part of the RF oscillator is connected to external frequency determining components via pins 2 and 6 of the IC. At the resonant frequency, the capacitive reactance, X_c, must be 70 Ω between pins 2-3 and pins 5-6, while X_c = 26 Ω must be observed between pins 3-5. The ground connection of the RF oscillator, pin 4, must be connected to the screening can of the inductor. An external oscillator signal may be applied to the TDA5664X via pins 2 and 6.

Table 1. Application circuit specification

Parameter		Min.	Max.	Unit
Supply voltage	U_s	4.5	5.5	V
Video input frequency	f_{VID}	0	6	MHz
Audio input frequency	f_{AF}	0	20	kHz
Output frequency	f_o	30	860	MHz
Operating temperature	T_a	0	70	°C
Subcarrier frequency	f_{OSC}	4	7	MHz

This signal may be coupled inductively or capacitively.

For optimum operation and minimum spurious radiation, the oscillator pins (2 to 6) must be screened from the modulator output pins (10, 11 and 12). The RF attenuation of this screening must be 80 dB or greater.

Application circuit

The circuit diagram of a TDA5664X-based UHF TV modulator is shown in Fig. 2. The balanced mixer outputs, pins 10 and 12, are connected to a wideband balanced-to-unbalanced (balun) transformer, which ensures a phase difference of exactly 180°. The basic construction of this balun on a two-hole ferrite core is shown in Fig. 3. The attenuation of the device must be smaller than 3 dB at the frequency of operation.

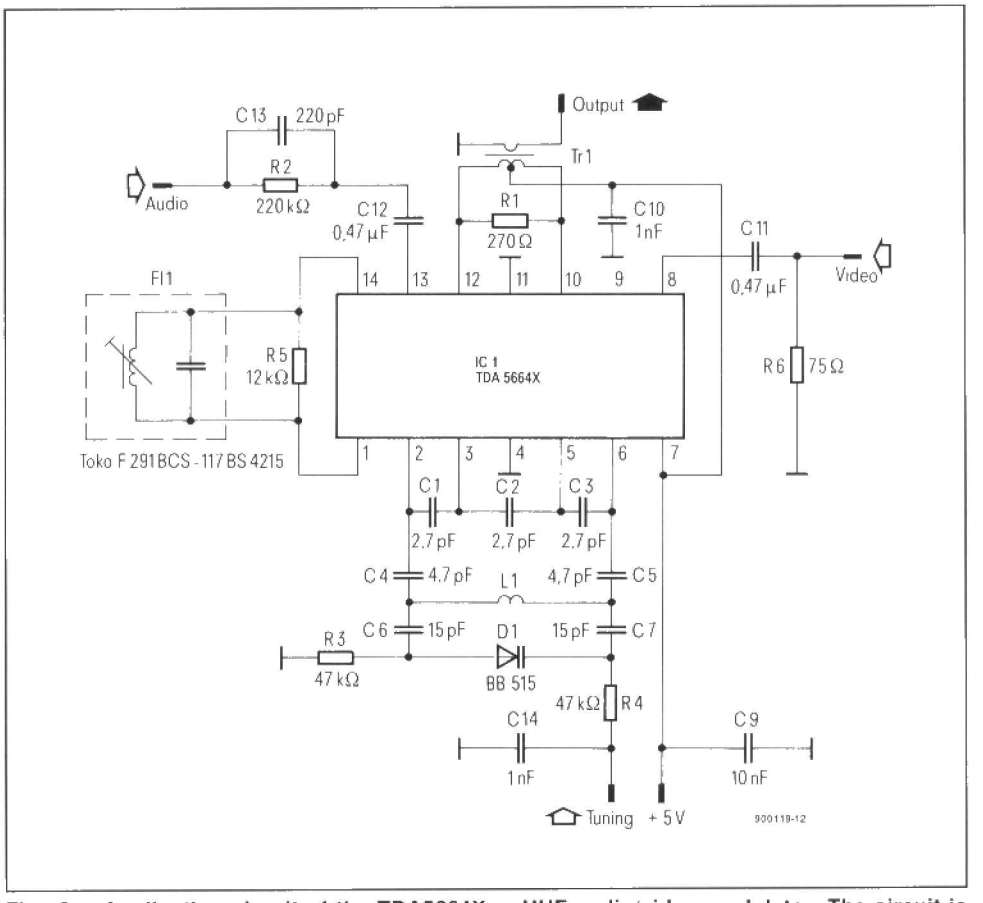
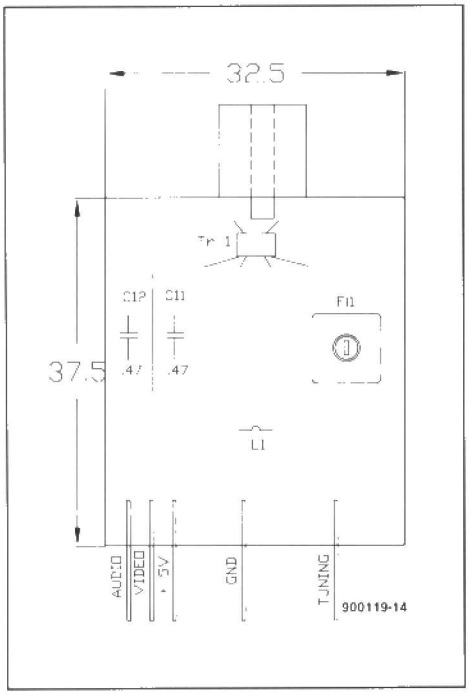


Fig. 2. Application circuit of the TDA5664X: a UHF audio/video modulator. The circuit is tuned to the desired TV channel by applying a tuning voltage to the varicap diode, D1.



Because of the impedance change from 270 Ω balanced to 50 Ω unbalanced, the RF output voltage of the modulator is about 1.5 times the RF voltage across R1. This is based on the assumption that the balun has an attenuation of 0 dB.

Finally, a suggested PCB design for the modulator based on the SMA version of the TDA5664X is shown in Fig. 3. The design of this PCB meets the requirements as regards decoupling and minimum stray inductance in the oscillator as well as the modulator output circuitry. The modulator is tuned to a TV channel between 30 and 40 (i.e., between 543.25 MHz and 623.25 MHz) by applying a voltage to the TUNING input. ■

Source:
Siemens Components issue 28 (3/90).

COMPONENTS LIST

Resistors (SMA):

1	270Ω	R1
1	220kΩ	R2
2	47kΩ	R3;R4
1	12kΩ	R5
1	75Ω	R6

Capacitors:

3	2pF7 SMA	C1;C2;C3
2	4pF7 SMA	C4;C5
2	15pF SMA	C6;C7
1	10nF SMA	C9
2	1nF SMA	C10;C14
2	470nF 5mm	C11;C12
1	220pF SMA	C13

Semiconductors:

1	BB515	D1
1	TDA5664X SMA	IC1

Miscellaneous:

1	B62152-A0008-X017 balun (Siemens)	Tr1
1	F291BCS-117BS4215 (Toko)	FI1

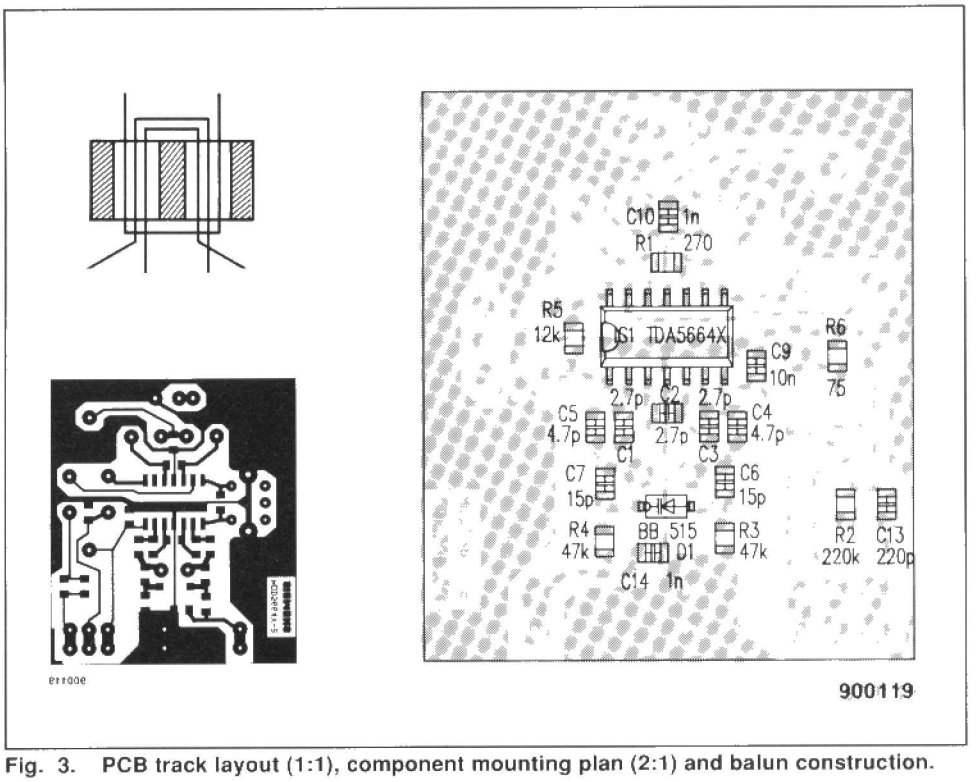


Fig. 3. PCB track layout (1:1), component mounting plan (2:1) and balun construction.

REAL-TIME CLOCK FOR ATARI ST

The Atari ST is a user-friendly computer supported by a massive amount of excellent software. Unfortunately, early models of the ST lack a clock circuit that keeps ticking when the computer is switched off. The circuit presented here overcomes this problem.

F. Dossche

ALTHOUGH the design of the Atari ST computer is modern by any standard, a real-time clock (RTC) is provided only on the latest models. This is surprising because the main rival of the ST, the IBM PC or compatible, has had an RTC as an option or a standard feature longer than many of you will care to remember. Owing to the absence of an RTC, many Atari ST users are forced to set the date and time, every time the computer is switched on. To help out the thousands of faithful owners of older ST models, we have developed a real-time clock that is inexpensive and simple to build.

One of the most attractive features of the Atari ST is the number of interfaces. One of these interfaces, the printer port, is used here to connect the real-time clock to the computer. We hasten to add that you will be able to use the printer as before, since the RTC is inserted between it and the Centronics port, for which only a very small modification is required.

Up-to-date with the RTC

Of the real-time clock ICs currently available, the MSM5832 from OKI and the MC146818 from Motorola are probably the best known and widest used. The Motorola IC has an advantage over the MSM5832 in offering an 8-bit wide databus, and a 50-byte non-volatile RAM (random access memory). The data retention is achieved with an external rechargeable battery.

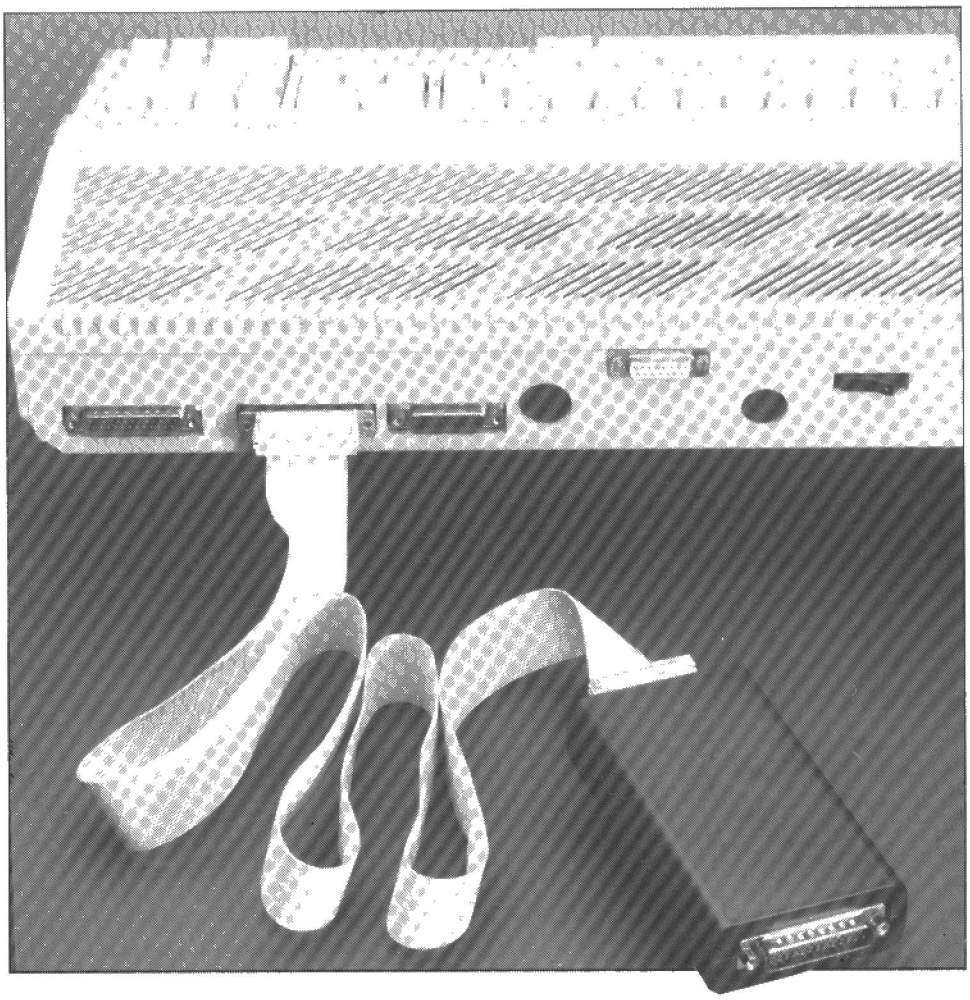
Here, the Motorola IC is used, although no use is made of its internal RAM. The 8-bit databus of the RTC chip allows the control software to be kept fairly simple, and in addition affords the possibility to implement further extensions circuits on the Centronics port. The control software for the present project is supplied on disk in the form of a source listing written in C. This program may be used as the basis for further hardware or software functions that you may wish to add. The hardware presented here, and the object code compiled with the aid of the C program, can be used to develop a 'desk accessory' to support the new clock function.

Returning to the hardware, the circuit diagram of the clock extension is shown in Fig. 1. The heart of the circuit is the RTC chip from Motorola. Besides four logic gates and two bistables, the circuit contains a handful of discrete parts used mainly to implement a battery back-up function for the RTC. The two bistables and one I/O line on the computer's main board serve to direct the data on the Centronics bus either to the printer or the real-time clock. In addition, one of the bistables indicates whether the 8-bit word sent to the clock circuit is intended to select an address location, or to be stored as data in the RTC.

The real-time clock sits between the Centronics port on the computer and the Centronics input of the printer. Hence, it has an input an output connector.

At the left in the circuit diagram we find connector K1 which links the circuit to the computer. Two new signals appear on this connector on pins 16 and 17. Pin 16, normally the $\overline{\text{RESET}}$ line, is not used by the Atari ST, and now carries the computer's 5-V supply voltage. Since the $\overline{\text{RESET}}$ signal is active low according to the Centronics standard, placing +5 V on pin 16 has no effect on the printer (anyway, the ST is not capable of issuing a reset via this line).

Pin 17 of K1 is connected to an unused I/O line in the computer, and serves to direct data either to the RTC or to the printer. The I/O line is found on pin 14 of the sound generator IC in the ST, the Yamaha YM-2149. Although not used in the hardware of the ST, this I/O line is supported by the BIOS (basic input/output system), which makes it perfect for the present application. Pin 17 on the Centronics connector is chosen because it is not used on the ST or the printer. Do, however, check that the cable between the computer and the RTC has a wire for the signal on pin 17. In general, most serial cables for



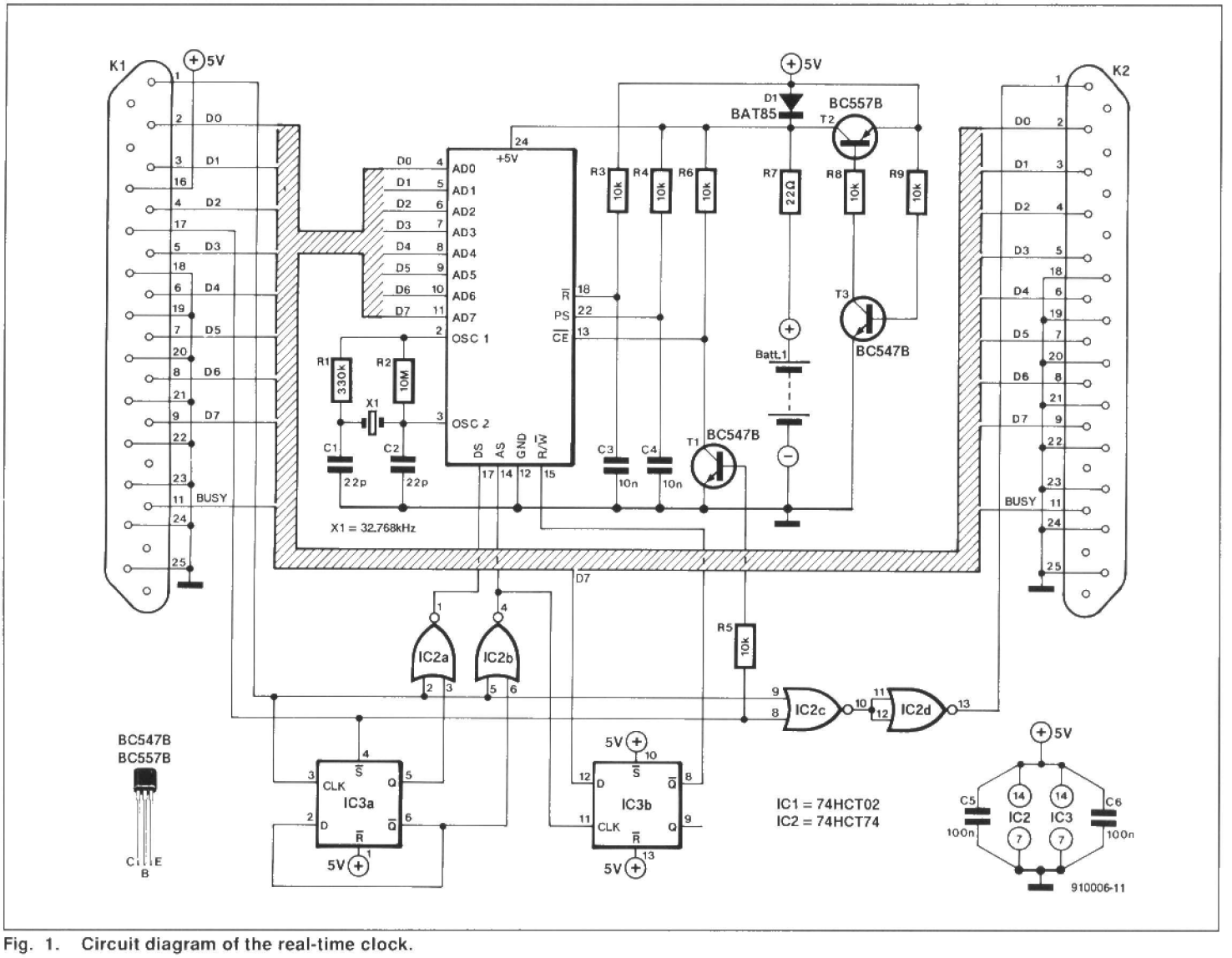


Fig. 1. Circuit diagram of the real-time clock.

PCs have a wire for each of the 25 pins, and will, therefore, meet our requirement. You may also decide to make your own 25-way cable, which has the advantage that it can be made shorter than most ready-made cables. These are usually 1 m or 2 m long, and quite bulky for our application. A home-made cable may be produced by a short length of 25-way ribbon cable terminated in an IDC-style male 25-way D-connector at one end, and a female D-connector at the other end.

Returning to the circuit diagram, the signal at pin 17 of K1 enables bistable IC3a by making the $\overline{S}$ line logic high. This results in any changes at the set and the reset inputs of IC3a being ignored, so that the bistable remains in the 'set' state because the SET line was active last. Also, the strobe signal for the printer (connected to K2) is blocked by gates IC2c and IC2d, and the enable input of the RTC is actuated via transistor T1. Next, an RTC address is passed to the circuit via the Centronics datalines. The most-significant bit, D7, indicates a read or a write operation to or from the RTC registers.

A pulse on the strobe line (pin 1 of K1) is fed to the AS input of the RTC chip via bistable IC3a and gate IC2b. This pulse is used to transfer an 8-bit word on the Centronics datalines to the RTC, or vice versa, as indicated by the level of databit D7. After the strobe pulse, the inverted level of D7 is applied to the R/$\overline{W}$ input of IC1. When the next strobe pulse occurs, IC3a toggles because the Q output of this bistable is connected to its D (data-) input. The pulse is subsequently fed to the DS (data strobe) input of IC1 via IC2a. Data may be read before the end of the second strobe pulse. When this is finished, the computer will de-actuate the 'select' line (pin 17 on K1). The printer can then be used again, and the clock operates. The above sequence is used to store the time and date in the RTC, and also to read these back into the computer, allowing the system clock in the ST to copy the RTC information. Gone are the days when you had to set the system clock every time the ST was switched on.

The rest of the circuit is fairly simple. The PCB has two options for charging the battery. The simplest is by means of diode D1. When the ST is switched on, the battery is charged via D1 and R7. The RTC is also powered via the diode. This must be a Schottky type to ensure a low voltage drop. Remember, the charge current can become too small when the computer supply voltage is on the low side, when the battery voltage is on the high side. This is prevented by a diode with a low voltage drop.

If you can not secure the BAT85 or an equivalent Schottky diode, add the circuit based on T2 and T3. When the computer is switched on, T3 starts to conduct and switches on T2. By virtue of the relatively low collector-emitter voltage of T2, the charge current for the battery is sufficiently high. When the computer is switched off, T3 blocks and turns off T2, so that the battery takes over the supply of IC1. Note that the transistor-based supply is an alternative to the single Schottky diode — components T2, T3, R8 and R9 are not fitted if you use a BAT85.

The $\overline{RESET}$ and PS inputs of IC1 are taken logic high briefly after the supply is switched on. This ends the low-power standby state of the RTC, and causes it to switch to normal operation.

A quartz crystal, X1, together with C1, C2, R1, R2 and two gates in IC2 form an oscillator that supplies a clock of 32.768 kHz to the RTC. This frequency is used in most battery-powered clocks and electronic wristwatches.

Construction

The construction of the real-time clock unit will present little difficulty if the printed-circuit board shown in Fig. 2 is used. Start the construction by fitting the wire links and the connectors. Note that K1 is a male type, and K2 a female type. If you swap them acciden-

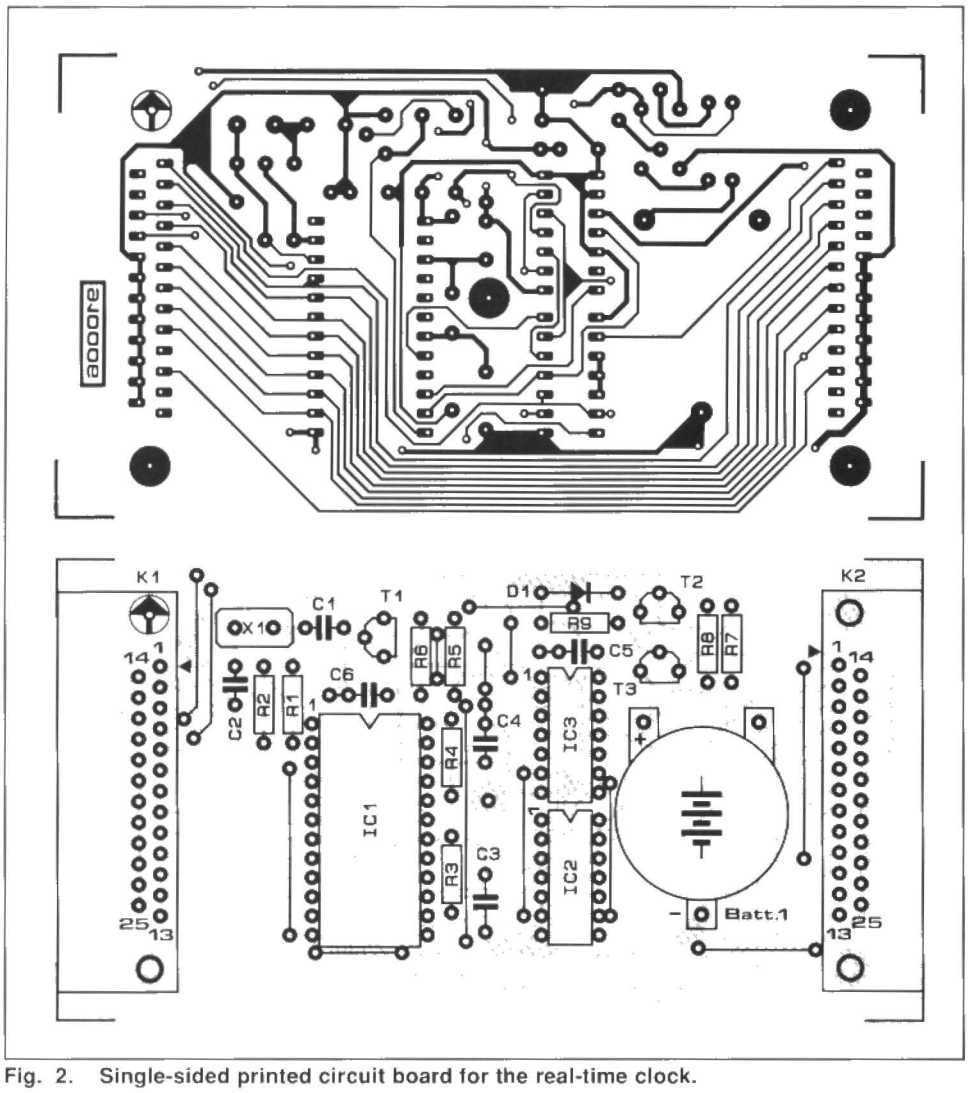


Fig. 2. Single-sided printed circuit board for the real-time clock.

tally, you will be unable to connect the circuit properly to the input and output cables.

Proceed with fitting the remaining parts on the board. IC sockets are not strictly required. If you do decide to use them, be sure to buy good quality types.

The completed printed circuit board fits into an ABS enclosure of dimensions 120×70×30 mm. The side panels of the enclosure are cut to allow the connectors to protrude.

A small modification is required in the computer before the RTC can be connected. Although the 'operation' is really no more than soldering two wires, it may still take you an hour or so to complete because the computer has to be disassembled. After removing the floppy disk drive and the switching power supply module, you should be able to see the printer connector and the Yamaha chip. Take the main board out of the enclosure, and remove the metal screen at

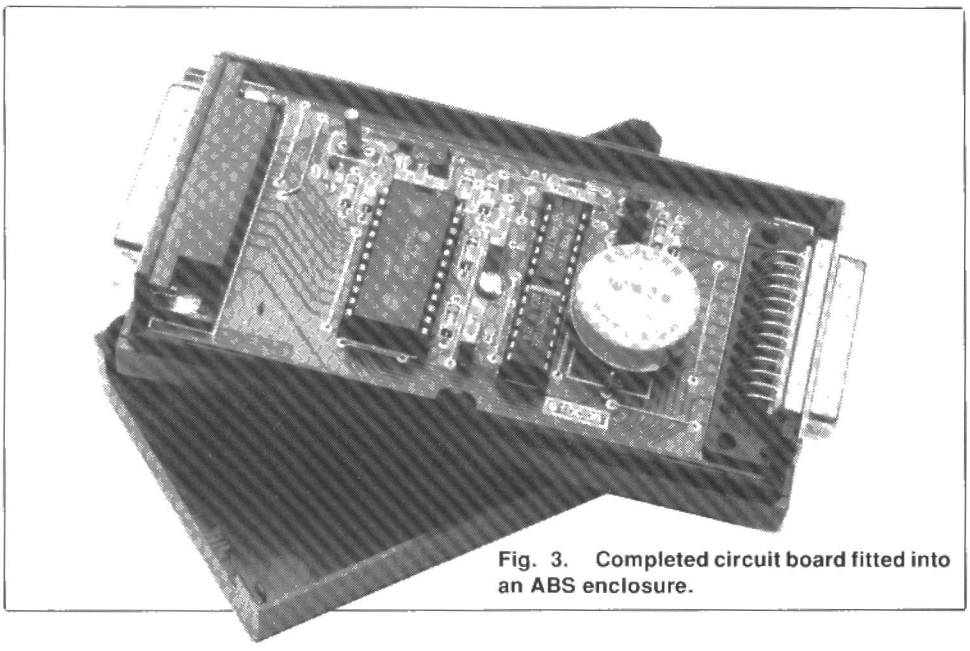


Fig. 3. Completed circuit board fitted into an ABS enclosure.

COMPONENTS LIST

Resistors:

1	330kΩ	R1
1	10MΩ	R2
6	10kΩ	R3-R6;R8;R9
1	22Ω	R7

Capacitors:

2	22pF	C1;C2
2	10nF	C3;C4
2	100nF	C5;C6

Semiconductors:

1	BAT85	D1
2	BC547B	T1;T3
1	BC557B	T2
1	MC146818	IC1
1	74HCT02	IC2
1	74HCT74	IC3

Miscellaneous:

1	25-way male sub-D connector with angled pins, for PCB mounting	K1
1	25-way female sub-D connector with angled pins, for PCB mounting	K2
1	32.768 kHz quartz crystal	X1
1	3.6V NiCd battery	Batt.1
1	ABS enclosure; size approx. 120×70×30mm	
1	Printed circuit board	910006
1	Diskette with control software	ESS1621

both sides. This means that you have to bend a couple of small metal brackets with the aid of tweezers. After turning the main PCB, you should have access to the sound generator connections. Run a wire from pin 14 of the Yamaha chip to pin 16 of the printer connector, and another wire from pin 40 of the Yamaha chip (+5 V) to pin 17 of the printer connector. This completes the modification. Re-assemble the computer.

Software

As usual, hardware is never complete without the appropriate software. The clock unit described here is supported by a control program on disk, which may be ordered through our Readers Services. The disk contains the ready-to-go desk accessory for the clock, as well as the source listing used to compile the machine code. As already mentioned, this listing is intended for those of you who want extra features for the clock, such as a programmable alarm. You may also want to use the 50-byte non-volatile RAM area in the RTC chip.

The source code can be converted into a control program with the aid of, for example, the Mark-Williams C compiler. This is not strictly required, though, since you can simply copy the control program on the floppy disk (supplied by us) to your system disk. Every time the computer is switched on, the program will automatically copy the RTC data to the system clock. Now, is that up-to-date or not? ■

STEPPER MOTOR BOARD

PART 1: PC INSERTION CARD AND CONTROL SOFTWARE

Getting a stepper motor to work properly invariably seems to require either a lot of discrete electronics, or an expensive dedicated integrated circuit. However, since the actual commands for stepper motors are almost always supplied by a computer, it is a challenging idea to economize on the hardware, and have the software do the work.

H. Kolter

STEPPER motor controls are available in many shapes and sizes, ranging from complex to ultra-simple, and based on a variety of integrated circuits, including the MC3479, the L297/298 and the TDA1024, all of which have been used in projects described in this magazine. By contrast, the control described here is not based on any of these ICs. None the less, it is versatile, simple to build and relatively cheap.

The circuit described has evolved as part of a PC-controlled professional milling machine that accepts CNC-format data to the Gerber standard. CNC stands for computer numerical control.

The concept

The above application was aimed at developing a complete milling machine for very accurate processing of aluminium, steel and plastic workpieces. When the project was initiated, there was the choice between (1) 'intelligent' motor control with relatively simple control software, and (2) a simpler controller with powerful, complex, software. To ensure the best possible results in regard of speed and accuracy of the system, the first option requires the motor control to be geared accurately to the specific features of the milling machine.

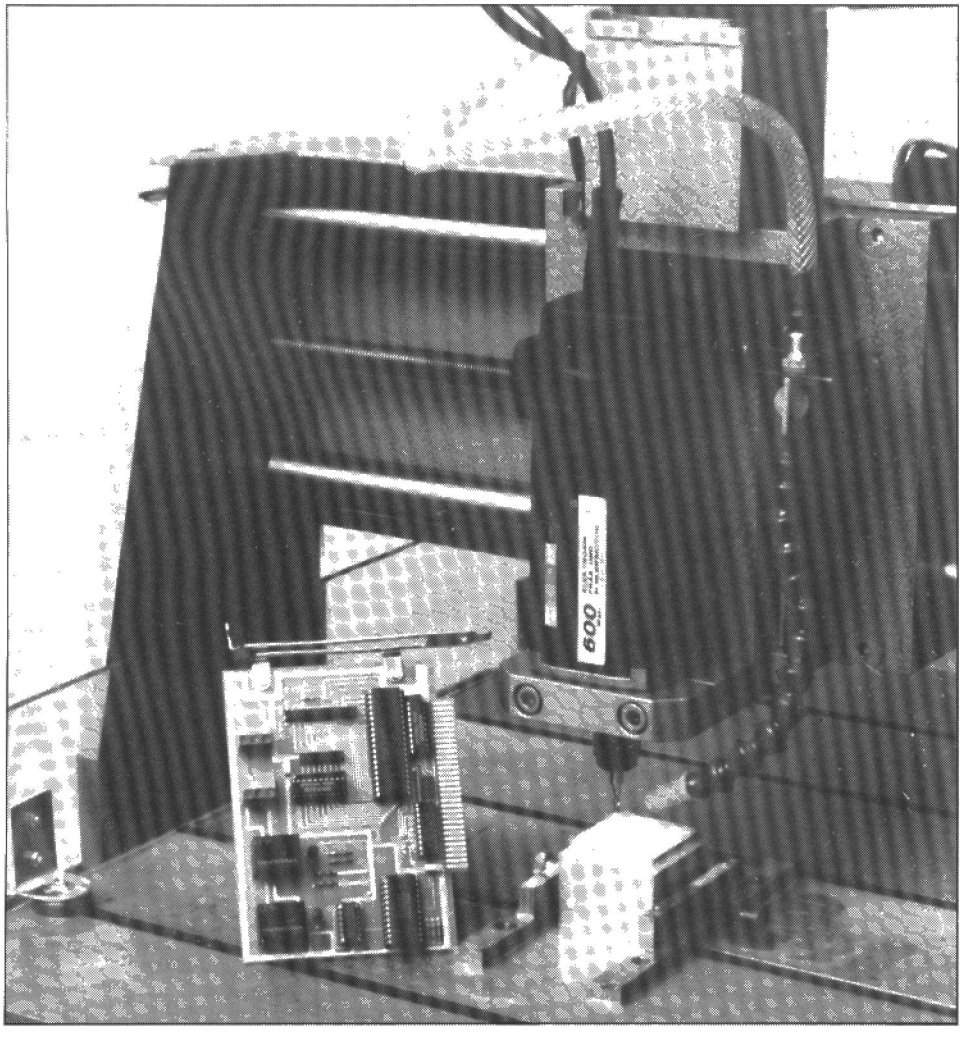
The second option has the advantage that changes to the machine, or extensions, are easier to support with appropriate software extensions. Since the electronics and the milling machine were developed roughly at the same time, the choice of the stepper motor control was clearly in favour of the second option: simple hardware and complex software.

In practice, the computing power required for the system can only be provided by a PC-AT or a compatible machine with a clock speed of at least 16 MHz. The computer program consists of an interpreter that reads drill and fraise data produced to the Gerber standard, and converts these into stepper motor commands.

The interpreter uses a configuration file that contains various system parameters such as the type of stepper motor (bipolar or unipolar, rotation per step, maximum step rate, etc.), and the main properties of the milling machine (spindle pitch, number of idle steps on spindle reversal, etc.). These parameters can be changed easily and allow the control system to be rapidly 'customized' for a particular application.

In line with the different functions, the electronics are divided into two parts. One part is an insertion card for IBM PCs, the other a larger board, which is fitted external to the PC, and contains the power drivers.

The PC insertion card described here is basically a digital I/O card based on the familiar 8255 PPI (programmable peripheral interface) from Intel. The 'half-size' insertion



card offers 24 input/output lines, and has an additional timer/counter IC Type 8253, a quartz oscillator and two relays. The quartz oscillator makes the timing of the I/O card independent of the computer speed. The two relays have changeover contacts and are suitable for switching mains loads.

The power driver board (to be described in part 2 of this article) has a fairly large power supply and 16 optocouplers that afford electrical isolation between the computer and the stepper motors. TTL buffers are provided between the optocouplers and the 16 power drivers. These buffers are also used to drive a LED-based readout that signals the active status of all stepper motor windings. The readout will be found particularly useful when a machine is first connected, or during program debugging.

Circuit description

The PC interface shown in Fig. 1 is a more or less standard design based on the 8255 PPI. Apart from the data and address signals, the extension card uses a few control signals on the IBM slot, $\overline{IOWR}$ which indicates write activity in the I/O memory area, $\overline{IORD}$ which has the same function form read operations, and, of course, RESET. The extension card is powered by the computer via the extension bus.

The datalines are buffered with a 74LS245 octal bidirectional driver. The buffered datalines are connected to the PPI (the 8255) and the PIT (programmable Interface Timer/counter; the 8253). A single PAL (programmable array logic), IC3, handles all address decoding. It uses address line A3 through A9 and the IORD and $\overline{IOWR}$ signals to generate chip select signals CS0, CS1, CS2 and CS3, and in addition the enable signal and the direction control signal for the databus buffer, IC2.

The I/O lines of ports A and B of IC1 are available on a double row PCB pin header, K2. Port C is connected to the outputs of the programmable timer, IC5. Connections PC4 and PC5 switch the two relays via darlington transistors T1-T2. In most cases, a value of 1 kΩ will be adequate for R5 and R6. These resistors may need to be made smaller, however, when the relays do not come on reliably. The minimum value of R5 and R6 is 330 Ω.

PPI line PC3 has a special use here as it is connected to an external emergency switch that stops the entire system. Normally, PC3 is held at +5 V by a pull-up resistor, R4. The two remaining port lines, PC6 and PC7, are not used here.

The internal block diagram of the 8253 counter/timer is shown in Fig. 2. The three 16-bit counters, numbered 0, 1 and 2, are identical and can be preset to count down. The counters operate independently and can be programmed separately. The counter values can be read from the 8253 without blocking the clock signal. The preset values are loaded with the aid of four control words stored in the control word register. Since this has only one address, two bits, SC0 and SC1,

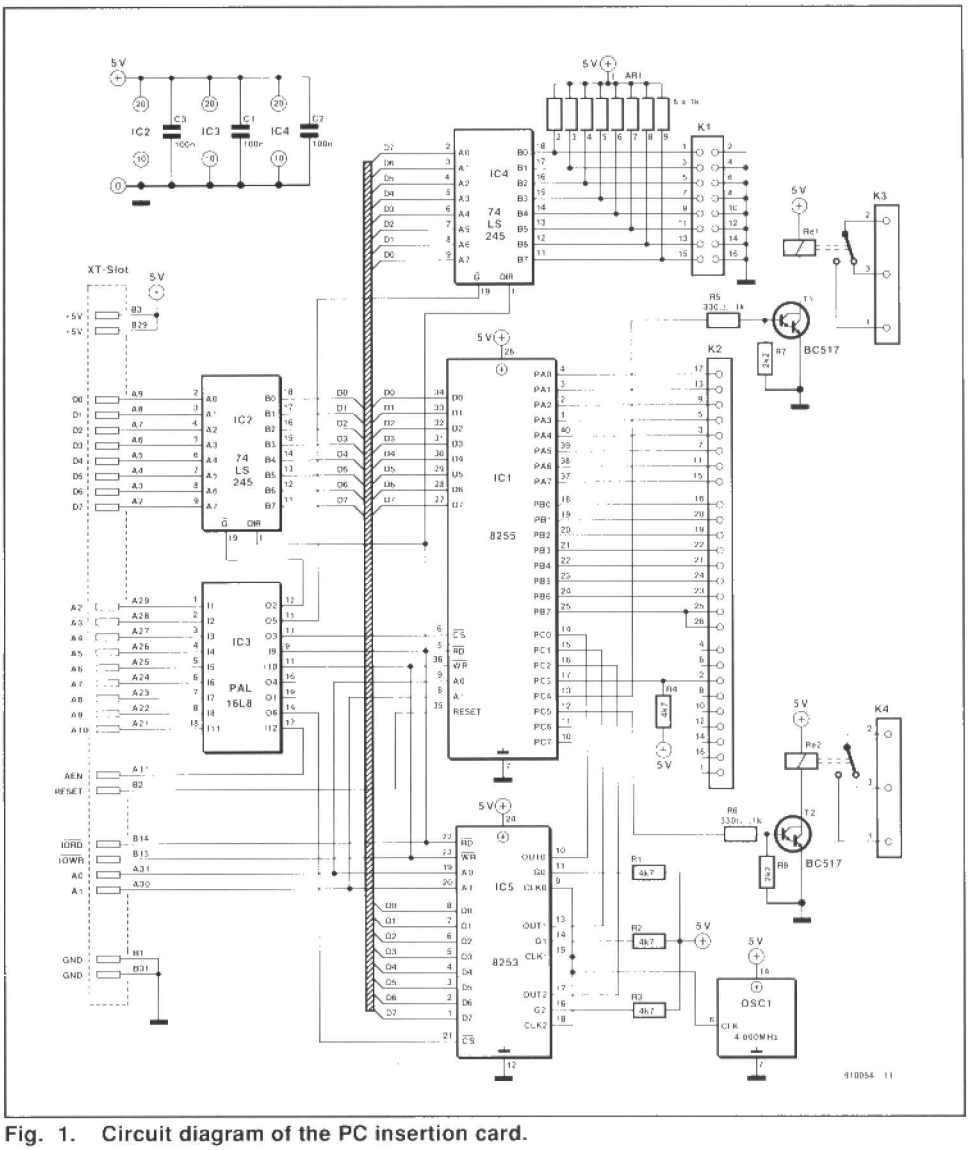


Fig. 1. Circuit diagram of the PC insertion card.

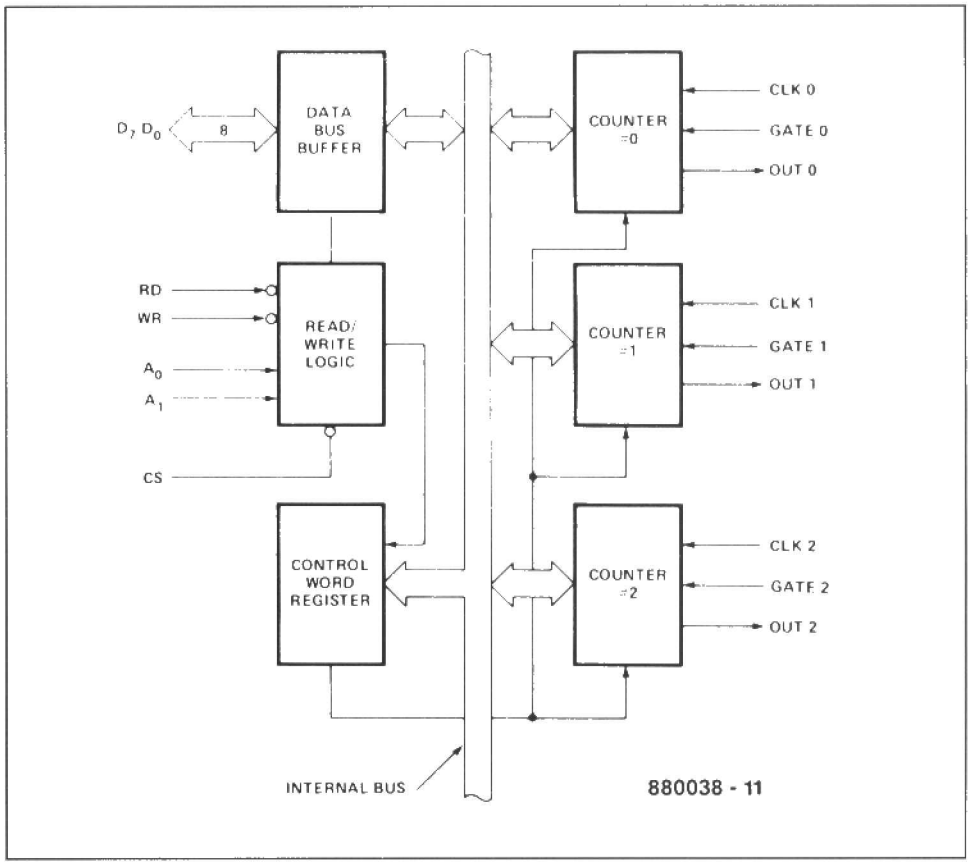


Fig. 2. Block diagram of the 8255 Programmable Peripheral Interface (PPI).

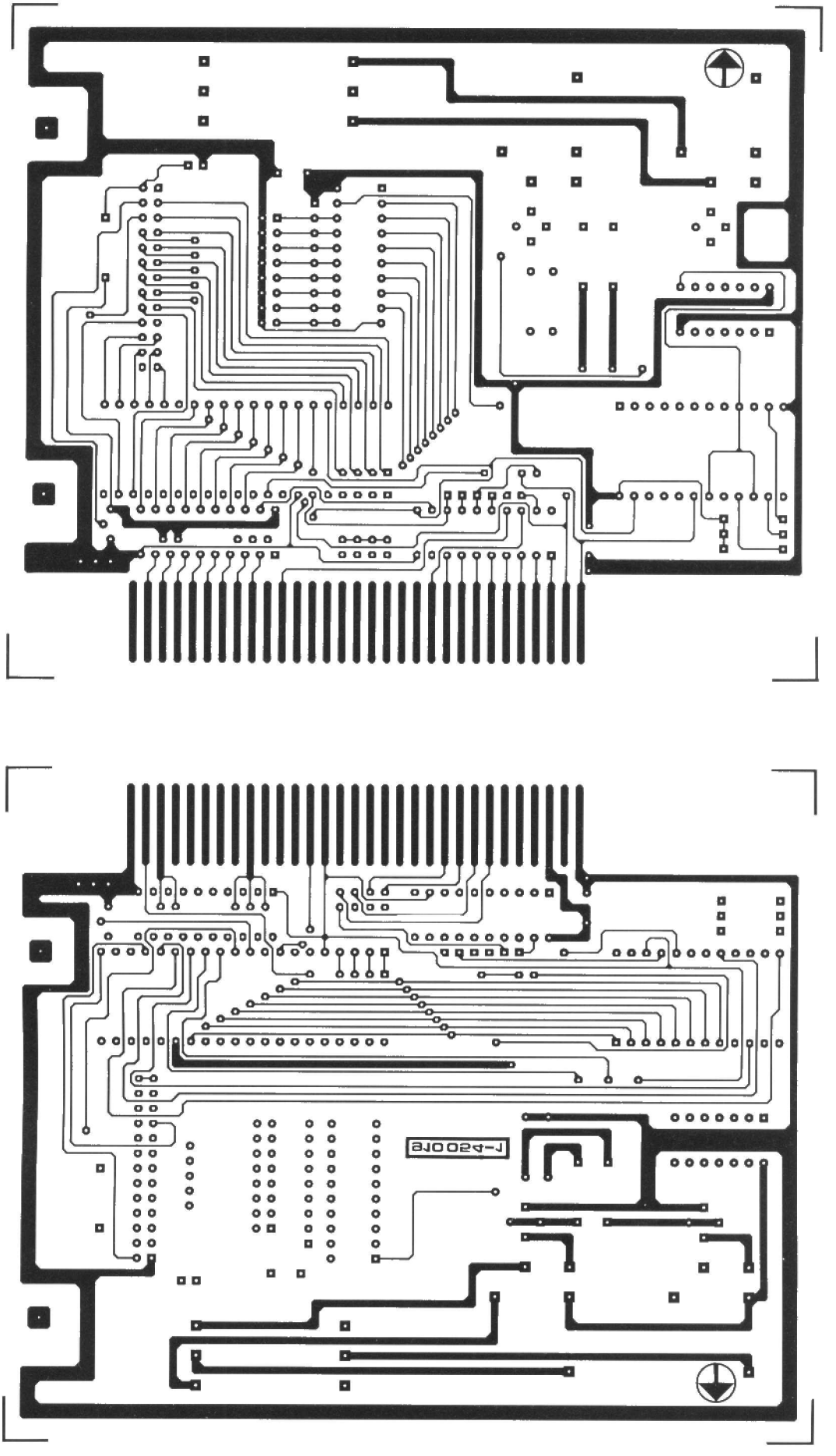


Fig. 3a. Track layouts of the component side and the solder side of the PC insertion card.

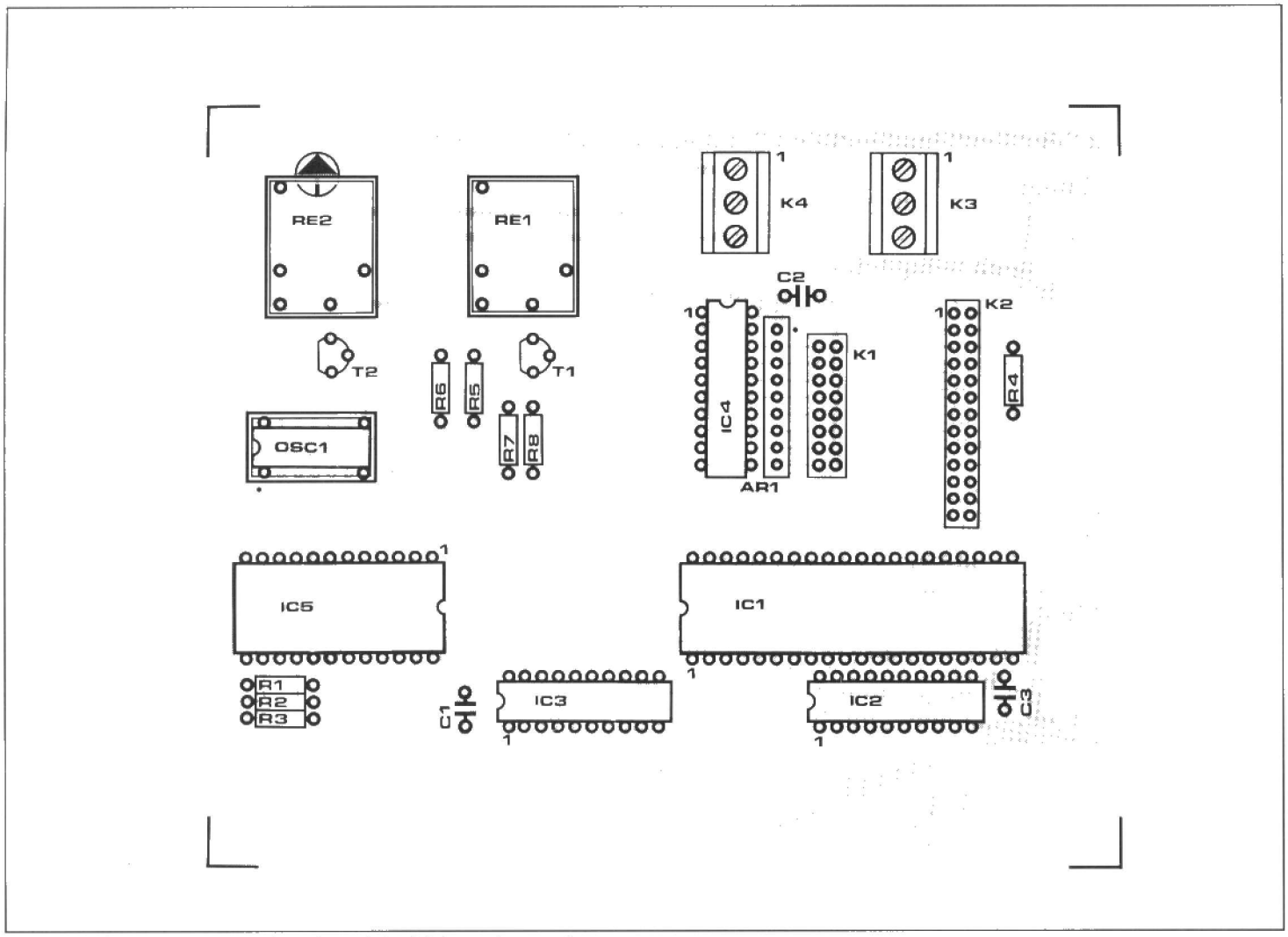


Fig. 3a. Component mounting plan of the PC insertion card.

COMPONENTS LIST

Resistors:

4	4kΩ7	R1 - R4
2	1kΩ (see text)	R5;R6
2	2kΩ2	R7;R8
1	8×4kΩ7 array	AR1

Capacitors:

3	100nF	C1;C2;C3

Semiconductors:

1	8255	IC1
2	74LS245	IC2;IC4
1	16L8 (ESS 6011)	IC3
1	8253	IC5
2	BC517	T1;T2

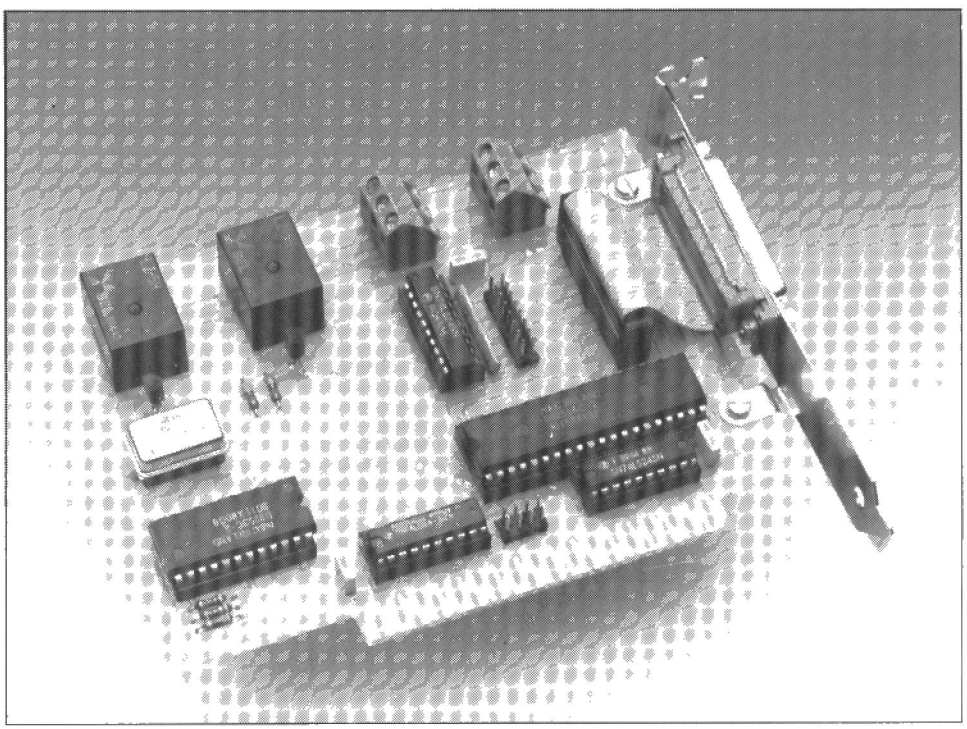
Miscellaneous:

1	4-MHz oscillator block	Osc1
2	PCB-mount 5V changeover relay	Re1;Re2
1	16-way 2-row PCB pin header	K1
1	26-way 2-row PCB pin header	K2
2	3-way PCB terminal block	K3;K4
1	printed-circuit board	910054-1

indicate the counter for which the control word is intended.

Returning to the circuit diagram in Fig. 1, the CLK0 through CLK3 inputs of the 8253 are supplied with a 4-MHz clock signal generated by oscillator block OSC1. All three gate (Gx) inputs of the counter/timer are tied to +5 V via pull-up resistors.

The 8253 is programmed to operate as a frequency divider. Depending on the preset value, a counter divides the oscillator frequency down to a particular value, for instance, 100 Hz, which is then passed to PPI port C. By loading different counter preset



values, the step duration of the stepper motors is made independent of the computer's speed.

IC4, a 74LS245, forms an 8-bit input port which is used to signal the status of a set of end switches fitted on the milling machine. The eight input lines of the port are held at +5 V with the aid of pull-up resistors. The end switches wired to K1 should, therefore, connect to ground when active.

The address assignment of the ports on the insertion card, and their functions, are summarized in Tables 1 and 2.

Construction

Populating the double-sided through-plated board (Fig. 3) should not cause difficulty. To make sure the card remains secure in the PC slot, you will need to secure it to a metal bracket as found on other insertion cards. Here, it is best to use (or make) a bracket with a relatively large vertical clearance that allows the two flatcables and the relay wires to pass.

Switch the computer off, fit the I/O card into a free slot, and secure the card to the metal frame at the rear of the PC. Switch on the PC, and check that a frequency of 4 MHz is present at pins 9, 15 and 18 of IC5. In case the PC will not boot up with the I/O card inserted, you are probably faced with a short-circuit on the board, or a faulty IC.

The data in Tables 1 and 2, and a few lines of BASIC or Pascal, allow the card to be checked for correct operation. For instance, reading address [base+8] (IC4) should return 1111 1111_2, which equals FF_H, or 256 decimal. Next, connect two or three jumpers to K1 to pull the input datalines logic low. Run the read test again, when the result should match the set bit pattern (a jumper produces a logic low).

Next, test the PPI by writing to the control register at address [base+3] ($0DE3_H$). Set all ports to output, then make all port lines logic high. The relays should come on.

The scope of this article does not allow a more detailed description of the way in which the 8255 and the 8253 are programmed. Fortunately, plenty of literature is available that covers the practical use of these ICs in great detail.

Software

A number of different, fairly complex computer programs are required before the fraising machine can be made to work. The first step in making a fraised product is to draw it with the aid of a CAD program, such as AutoCAD or AutoSketch, and save the drawing file in the DXF format. Next, a program called AutoPack-II is used to convert the DXF file into a format suitable for further processing. AutoPack-II is a 2½-dimension version of the 3-dimension program AutoPack. None the less, AutoPack-II allows you to view the workpiece in 3-D to the ISO standard. Also, all side views of the workpiece can be displayed at the same time, and the program is capable of calculating the curve described by the fraise. This curve is called fraise equidistant because the radius of the fraise itself is taken into account.

The fraise file generated by AutoPack-II consists of a set of so-called Gerber commands. The actual control software for the milling machine is a converter called CNC-DIN. Written in C, it reads the Gerber data and converts these into commands for the stepper motor board described here. CNC-DIN is available from the author, and allows you set a number of parameters related to the hardware. These parameters include the type of stepper motor used (2-phase or 4-phase), the number of steps per revolution, etc. The parameters and their settings are stored in a configuration file that can be modified as required for your own hardware. Figure 4 lists the G (Gerber-) functions to DIN-66025 that are supported by CNC-DIN. ⌟

Part 2 of this article will describe the motor driver board. Tables 1 and 2 mentioned here will be included in Part 2.

G routines supported by CNC-DIN
All dimensions in mm, DIN 66025.

Example of Syntax:
10 G00 x17.34 y200.0
20 G01 x10.90 y20.90

%	start of program
	remark
G00	Target point direction characteristic (x, y, z). Move to target point. Fraise carrier speed.
G01	Straight interpolation of target point (x, y, z). Fraise from current point to indicated target point. Fraise speed.
G02	Circle interpolation, clockwise. (xakt, yakt, x, y, i, j) current point (xakt, yakt), target point (x, y), centre of circle (i, j). Fraise an arc based circle information, from current point to target point.
G03	Circle interpolation, anti-clockwise. See G02.
G04	Spindle idle time. (f) idle time in seconds.
M58	Switch of spindle motor relay.
M59	Switch on spindle motor relay.
M08	Switch on pump for drill coolant.
M09	Switch off pump for drilling coolant.
G90	All absolute data.
G91	All incremental data.
G94	Spindle shift speed in mm/min. (x, y, z) speed indication for single spindle.
M30	end of program.

Fig. 4. Overview of Gerber commands supported by the CNC-DIN converter program.

Note:
The program CNC-DIN mentioned in this article is available from Kolter Elektronik • Steinstrasse 22 • W-5042 Erfstadt • Germany. • Telephone: +49 (2235) 76707, Fax: +49 (2235) 72048.

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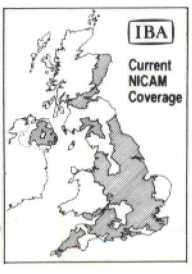

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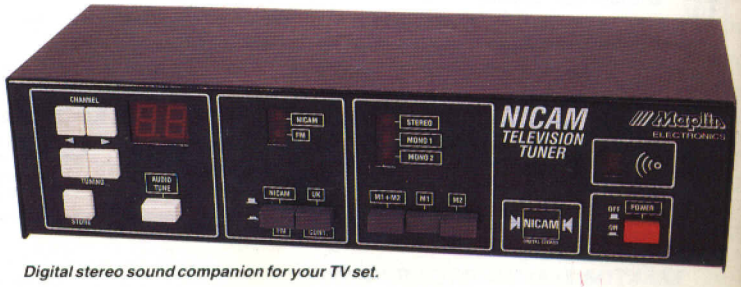

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